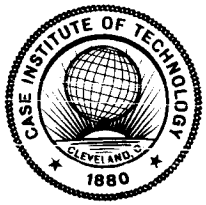

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DIGITAL SYSTEMS LABORATORY

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THEORY AND DESIGN TECHNIQUES FOR MAGNETIC-CORE MEMORIES

Vol II of II

by

Stuart F. Daniels

Harry W. Mergler
Professor of Engineering
Principal Investigator
NsG 36-60

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CHAPTER 5

PRACTICAL MEMORY CONFIGURATIONS AND OPERATION

5.1 Introduction[1, 2]

The linear selection memory and the coincident-current memory described in the last section of Chapter 3 are the two most common forms of magnetic-core memories. The CCM is historically older and more popular than the LSM, particularly when a large word capacity is required because of the simplified decoding logic. The LSM, on the other hand, is usually used for small memories because the external circuitry, exclusive of the decoding logic, may be less costly than for a comparative CCM. Also the LSM offers higher speed capabilities than the CCM because there is no upper limit on the magnitude of the read current which allows much faster switching times for a given core.

5.2 CCM Considerations

5.2.1 Typical CCM Bit Plane Geometry

A practical CCM is functionally the same as the one described in Chapter 3; however, the bit planes are usually wired in a different fashion to reduce noise in the output as well as to simplify the task of wiring.

Noise in the output may come primarily from four sources:

(1) partially selected cores - in an ℓ by m bit plane there will be $\ell + m - 2$ cores which will receive only one-half read current during a read operation. If a partially selected core produces 5 mv of noise, then the combined noise of several partially selected cores may add to produce a signal of great magnitude than a UV_1.

(2) mutual magnetic coupling between the drive wires and the sense winding - if a length of the sense winding is parallel to a drive wire the rapidly changing electromagnetic field produced by the rapidly changing currents in the drive wire will induce voltages in the sense winding.

(3) pick-up external to the memory array due to spurious signals in the surrounding media.

(4) stray capacitance between drive wires and the sense winding[3] is unavoidable and in large memories it may be considerable. Its effect is to produce a common-mode signal at both terminals of sense winding; that is, both terminals experience equal voltage excursions relative to ground. This does not add or subtract from the signal from the core, and it may be elliminated by using a sense amplifier with a high degree of common mode rejection.

Sense windings are usually wired keeping the following points in mind which minimize noise.

(1) If the sense winding is strung so that when any row or column is excited, half of the cores in that row or column induce positive voltages in the sense winding and the other half induce negative voltages, then the noise produced by one core will be cancelled by the noise produced by another core. However, there will be 0, 1, 2, 3or 4(depending upon the dimensions of the array) cores which will produce noise that will not be cancelled by another core as is shown in the Appendix. This will cause information signals to be of either polarity depending upon the selected core which will have to be considered in the design of the sense amplifier.

(2) If the sense wire makes an angle of 45 degrees or more with a drive wire, the mutual coupling between the two will be minimized.[3]

(3) If part of the sense winding is parallel to a given drive wire over a distance L, another section of the sense winding may be run parallel to the same drive wire--but in the opposite direction--over a like distance L, the signal produced in one length will then cancel with that produced in the other length, and the net mutual coupling is zero.

(4) If the sense winding forms a twisted pair between the bit plane and the sense amplifier, then a minimum of noise will be picked up external to the memory array. This is most conveniently done when the point of entry and exit of the sense winding in the bit plane are physically close to one another.

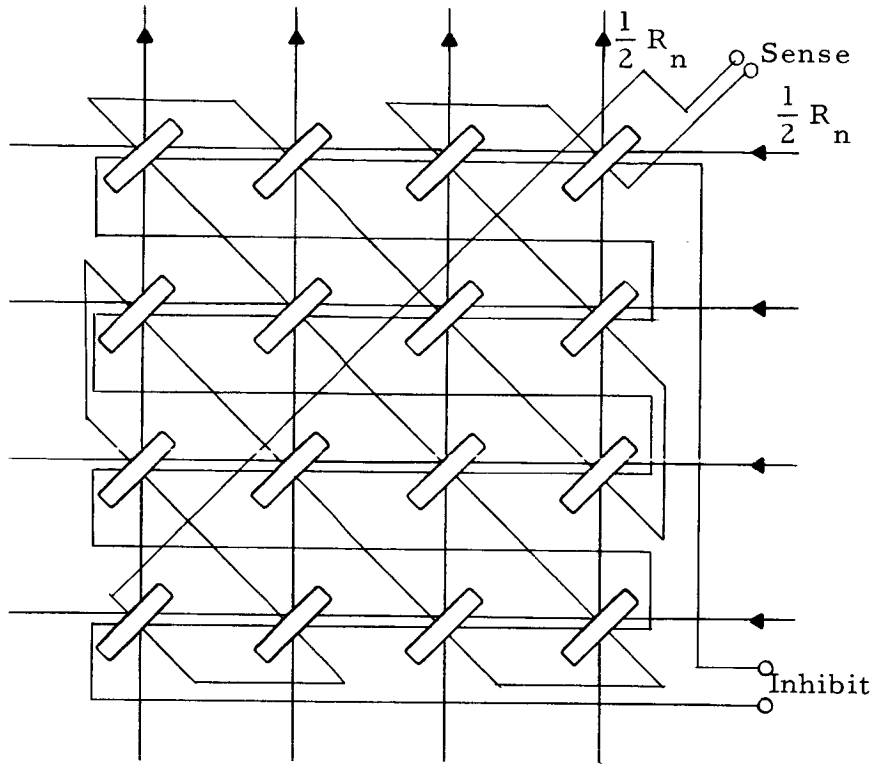
Three methods of sense winding wiring are now discussed.

(1) Simple Diagonal Sense Winding

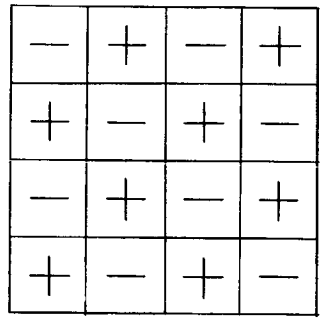
This is a conceptually simple sense winding illustrated in the 4 by 4 bit plane of Figure 5-1. The sense winding which starts at the upper right-hand corner and is threaded in a simple S fashion through every core in the bit plane and diagonal to all drive wires inside the matrix. It ends at the lower left-hand corner and is brought diagonally across the matrix back to the upper right-hand corner where a twisted pair is formed which goes to the sense amplifier. There is some mutual coupling, which is not cancelled, with every drive wire where the sense winding reverses direction; this limits the methods use to fairly small bit planes.

Because the sense winding passes through alternate cores in any row of column in opposite directions, alternate cores in any row or column produce signals of opposite polarity. This

(Arrows show proper direction of read current.)



(a) Wiring



(b) Relative polarities of signals produced by core on sense winding due to read excitations

Fig. 5-1 4 x 4 Bit Plane with Noise Cancelling Sense Winding

may be verified by following the sense winding through the array and applying the dot convention to each core encountered. Figure 5-1b indicates the relative polarities of the signals produced by each core during a read operation.

It should also be noted that the proper direction of the read and write currents is the same as in Figure 3-15, and the inhibit winding is therefore the same. The other wiring schemes to be described yield a simpler manner of threading this wire.

Finally it is observed that this method of wiring may be readily extended to any rectangular array.

(2) Double Diagonal Sense Winding [1, 3, 5]

This scheme, illustrated in the 8 x 8 bit plane of Figure 5-2a, may be used in any square bit plane where the number of cores on a side is divisible by four. This includes the common case where there are 2^{2n} words, and the bit planes are square with 2^{n} cores on a side. (This gives a maximum of decoding efficiency when the address is in natural binary form and contained in a 2n-bit register).

It will first be observed from Figure 5-2a that each core is at right angles to the adjacent ones in its row and column.

(Arrows show proper direction for half-read currents.)

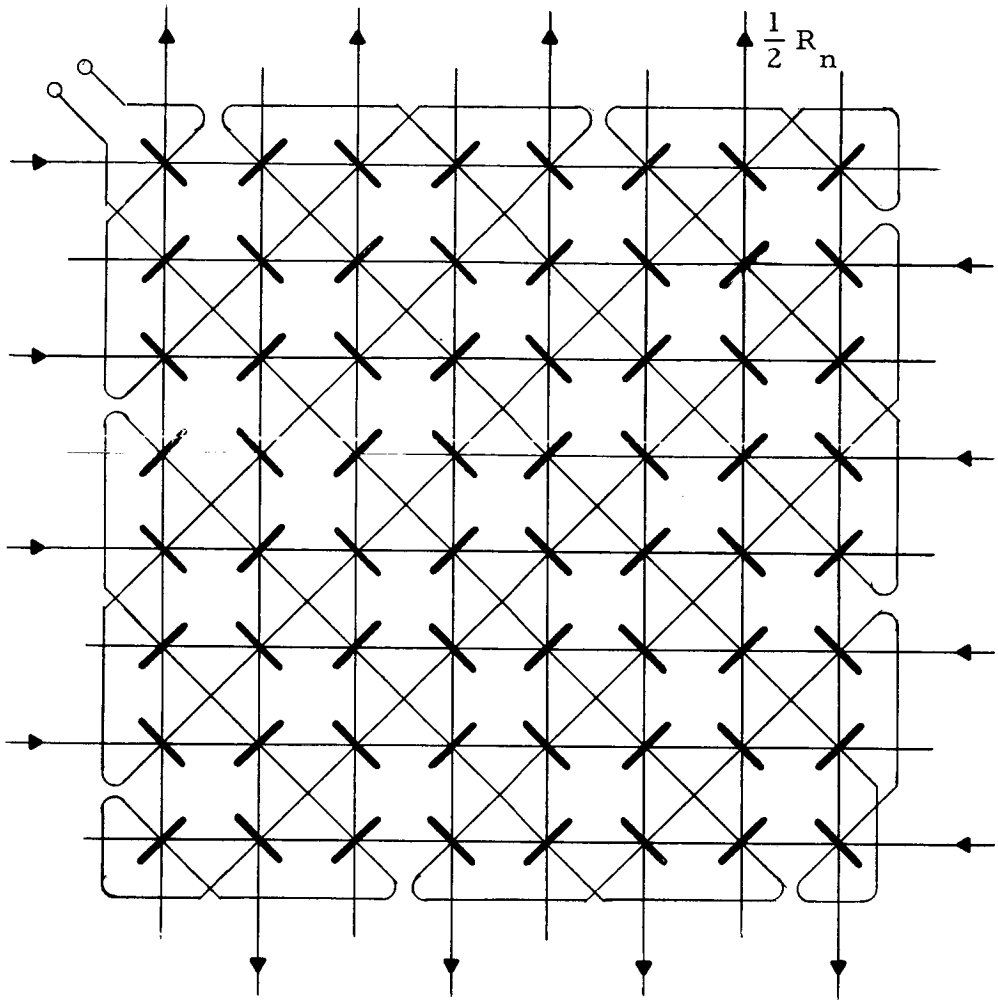


Fig. 5-2(a) Double Diagonal Sense Winding

	1	2	3	4	5	6	7	8
1	−	+	+	−	−	+	+	−
2	+	−	−	+	+	−	−	+
3	+	−	−	+	+	−	−	+
4	−	+	+	−	−	+	+	−
5	−	+	+	−	−	+	+	−
6	+	−	−	+	+	−	−	+
7	+	−	−	+	+	−	−	+
8	−	+	+	−	−	+	+	−

Fig. 5-2(b) Polarity of Signals Produced by Cores on the Sense Winding in Fig. 5-2 upon Read Excitation

This necessitates that the proper directions of write and read currents in adjacent rows and columns are opposite to each other (as is indicated in the Figure) in order that two partial select currents will add (rather than cancel) as they pass through the addressed core. This also allows the inhibit wire (which must pass through every core in a direction such that the current it carries is in the same direction as a half-read current) to be wound in the simple fashion shown in Figure 5-3.

Referring to Figure 5-2a, the sense winding is always diagonal to the drive wires inside the matrix as was the case in Figure 5-1. However, when it leaves the matrix (from a row or column) it skips a core (or a diagonal) before returning. When a corner is reached, the winding reverses direction through the corner core and continues. It is observed that the point of entry is physically close to the point of exit and a twisted pair may be readily formed. Furthermore because the sense winding closes on itself, the point of entry and exit may be at any corner or along any boundary as might be desired.

It will also be observed that any mutual coupling that occurs when the wire is external to the array is cancelled at some other point along the same side.

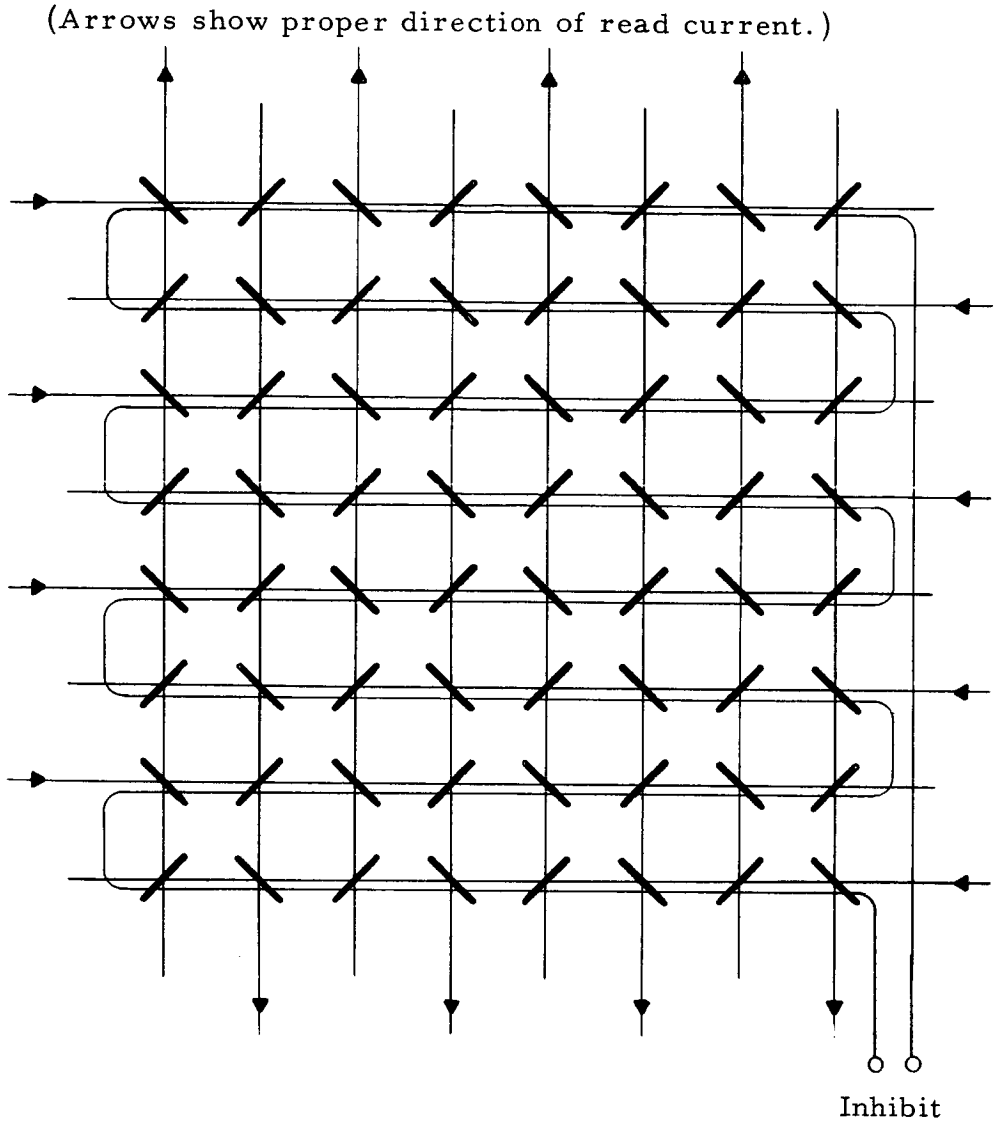


Fig. 5-3 Method of Wiring Inhibit Winding for use with Sense Winding of Fig. 5-2.

Figure 5-2b shows that the relative polarity of signals produced by the cores on the sense winding is in a double checkerboard pattern; along any row or column adjacent pairs of cores produce voltages of opposite polarity.

A rectangular bit plane of dimensions 4m x 8m (where m is any integer) can be constructed by considering it as two 4m x 4m planes, using a separate sense winding for each, and then connecting the two sense windings in series. This is illustrated for a 4 x 8 bit plane in Figure 5-4, and the method will work for the case when there are $2(2^n)^2$ addresses coded in binary and stored in a 2n + 1 bit register.

This is a common and widely used form of wiring, and bit planes wired in this or a very similar fashion are commercially available.

(3) Rectangular Sense Winding[3]

Figure 5-5 illustrates a 6 by 8 bit plane with a rectangular sense winding which is applicable to bit planes which have either an even number of rows or columns. The sense wire is run parallel to the horizontal (or vertical by changing the orientation) addressing drive wires. It follows a particular drive wire half way

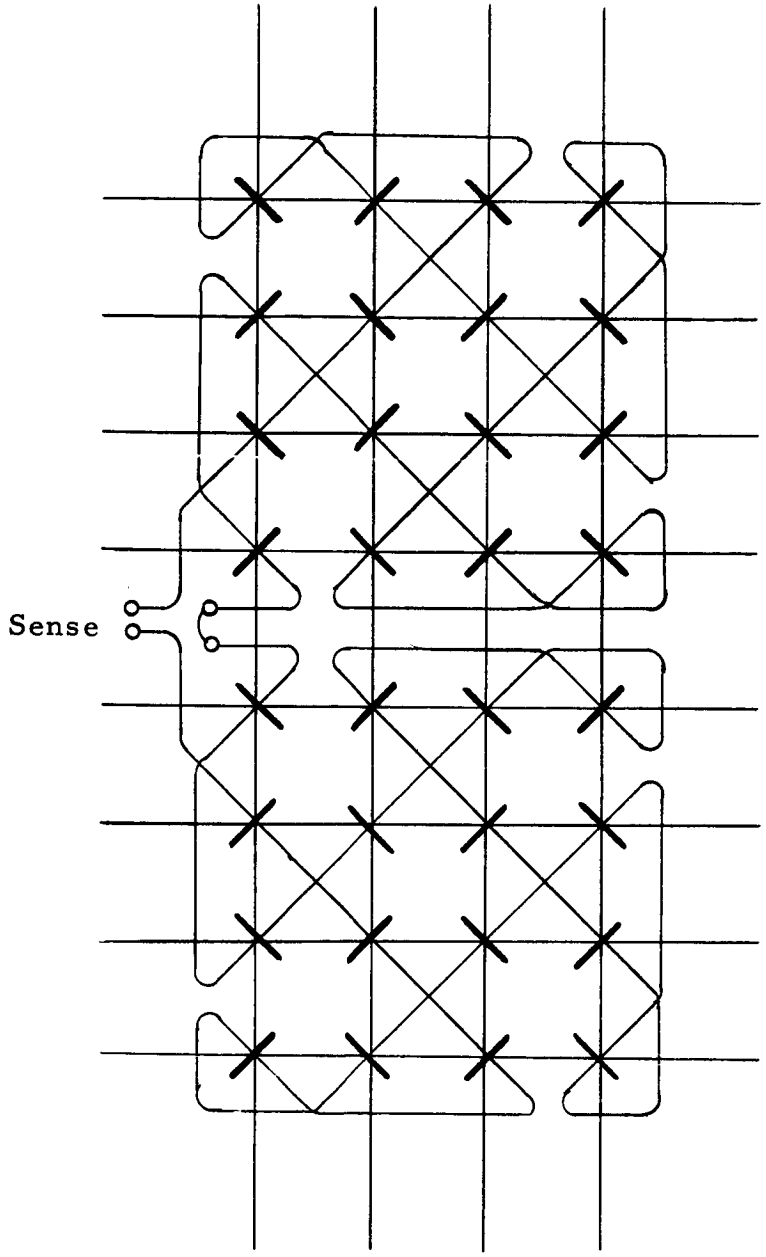
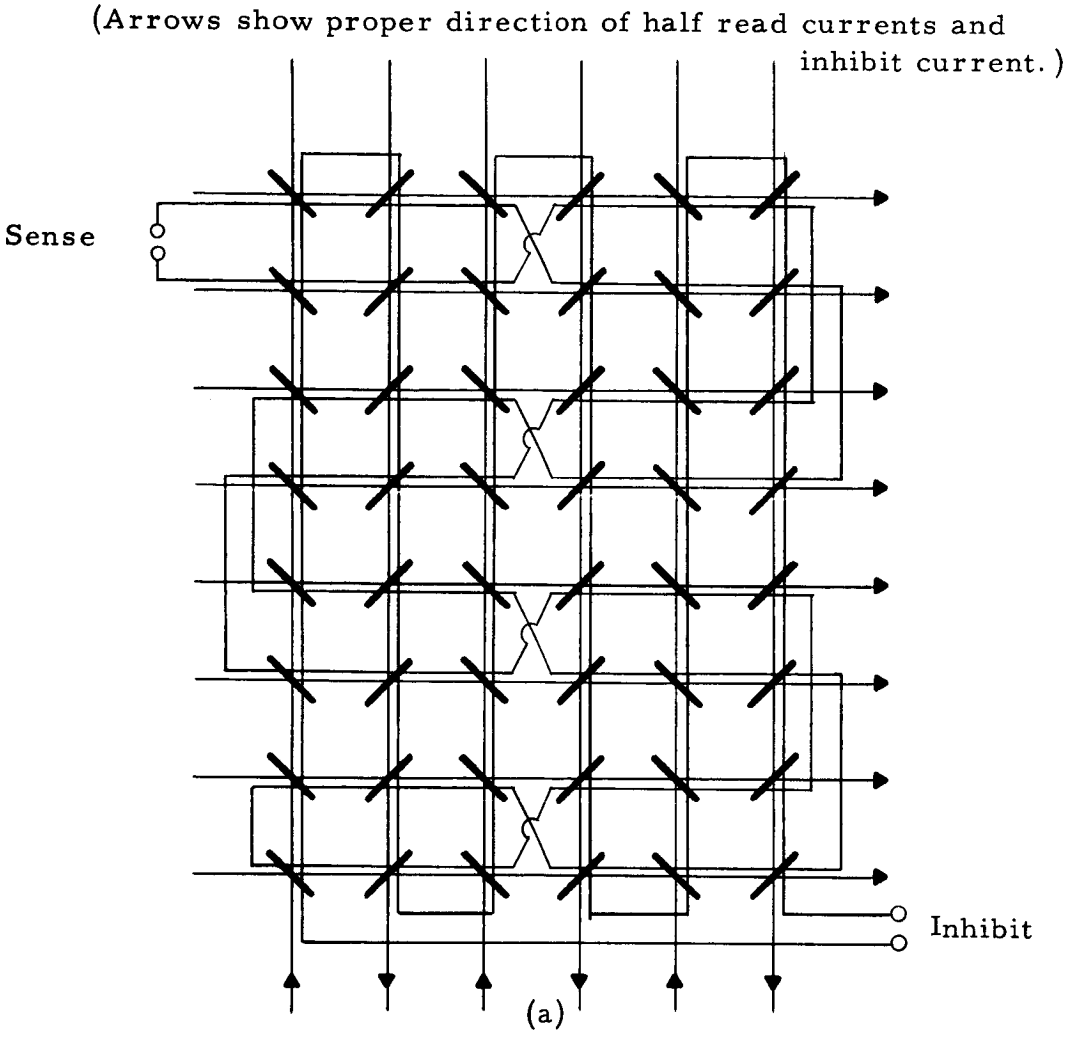


Fig. 5-4 Method of Extending Double Diagonal Sense Winding to a Rectangular 4m x 8m Bit Plane



+	+	+	−	−	−
−	−	−	+	+	+
−	−	−	+	+	+
+	+	+	−	−	−
+	+	+	−	−	−
−	−	−	+	+	+
−	−	−	+	+	+
+	+	+	−	−	−

(b) Relative polarity of core voltages

Fig. 5-5 Rectangular Sense Winding

through the array and then crosses over to the adjacent wire. When it emerges from the matrix it skips a row before returning in the opposite direction. It starts in one corner, and when it reaches the other end of the array it reverses and picks up the remaining cores, returning to a point adjacent to the starting point. By so doing, all mutual coupling is essentially cancelled. Like the second sense winding discussed, it forms a closed path and may therefore be started and terminated at any point.

The proper direction for addressing currents is the same in all drive wires parallel to the sense winding as shown. However, the cores have been arranged so that the direction of addressing currents in the other direction alternates in order that the inhibit winding may be wired in the simple fashion shown.

The resultant pattern of relative polarities of signals is shown in Figure 5-5b, and it is observed that core noise voltage will tend to cancel as desired.

5.2.2 Sense Output of a CCM Bit Plane

Even though the sense winding of a CCM is wired for a maximum of noise cancellation there will always be some noise.

First of all, there will always be considerably stray capacitance between the sense winding and the various drive wires, giving rise to the common mode problem previously mentioned.

Of much greater importance is the fact that partially selected cores will still produce noise for two reasons:

(1) There will always be partially selected cores whose voltages will not cancel with that of any other core.

(2) Due to differences in remanent flux, no two partially selected cores produce exactly the same output, and noise cancellation between two cores cannot be complete.

The number of noncancelling, partially selected cores in an l x m bit plane may be readily calculated (as is done in the Appendix), and the result is dependent upon whether l and m are odd or even numbers and the location of the addressed core. Furthermore, the polarity of the signal produced by a noncancelling core is always opposite to that of the information signal generated by the addressed core. Table 5-1 gives the number of noncancelling cores in an l x m bit plane. Notice that in the usual case, where both l and m are even there are always two noncancelling cores.

Table 5-1

Number of Partially Selected Cores in an ℓ x m bit plane--with a cancelling sense winding--whose noise voltages are not cancelled.

ℓ	m	Number of Noncancelling Cores
even	even	2
odd	even	1 or 3
even	odd	1 or 3
odd	odd	0, 2, or 9

Incomplete cancellation of the noise voltages produced by the remaining partially selected cores is due primarily to the fact that each core has a different past magnetic history, and its voltage response to a half-read current is a function of that history. These are small voltages that occur with the rise of the current and are of the shape indicated in Figure 4-3b. For a given rise time, the peak value of the voltage from one core depends mostly upon the change of flux that occurs, which in turn depends upon the initial remanent flux.

For example, a larger change of flux occurs when a partially selected core contains an undisturbed one than when it contains a disturbed one as evidenced by Figure 4-2. Hence, the

noise produced by a partially selected core containing an undisturbed one is greater than that produced by a core containing a disturbed one. A core containing a disturbed zero produces more noise than a core containing an undisturbed zero. In general, a given core will have received many partial excitations between the times it is addressed and will not be in exactly a disturbed or undisturbed state. Under these conditions it has been impirically found that the greatest difference in noise voltages occurs between a core containing a one whose last excitation was a half-write current (write disturbed one) and a core containing a zero whose last excitation was a half-read pulse (read disturbed zero).[3, 4] Hence, the least cancellation or maximum noise will occur when in the addressed core's row and column all of the cores generating noise of a given polarity contain write disturbed ones and all of the cores of the opposite polarity contain read-disturbed zeros.

As mentioned previously, the information signal from the addressed core may be of either polarity, and as a result the sense output of the bit plane is normally full-wave rectified before in the sense amplifier before it is decided whether the addressed core contained a one or a zero. Figure 5-6 indicates the rectified bit plant output when a one is read and when a zero is read. By

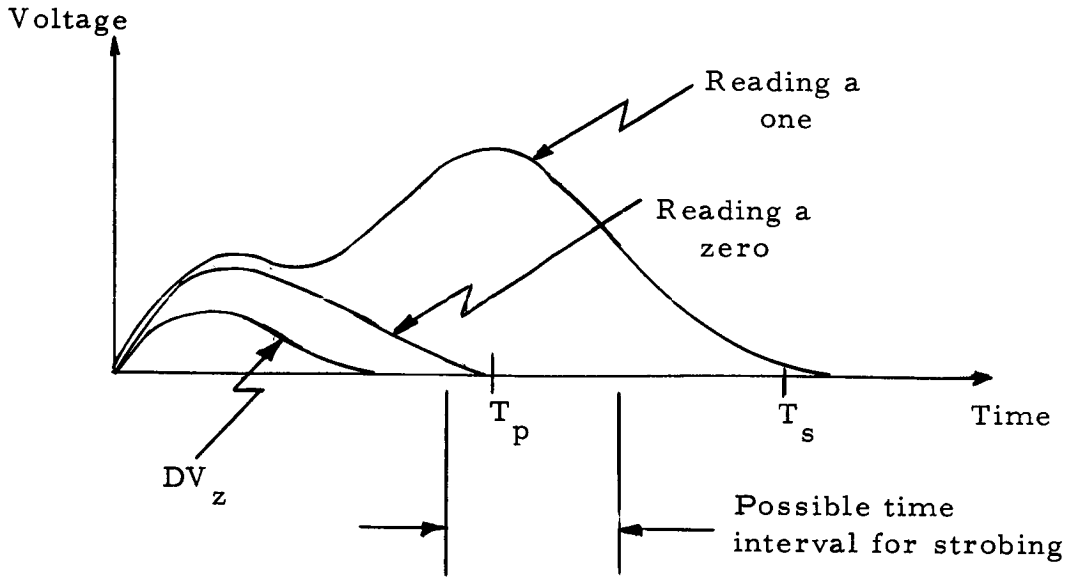


Fig. 5-6 Example of the Full Wave Rectified Output of a Bit Plane

way of comparison a typical DV_Z is also shown. It is seen that amplitude discrimination between a one and zero would be difficult to make as a result of the noise. However, since most of the noise and the zero output of the core occurs before T_P, amplitude discrimination may be made at that time by strobing the sense amplifier, and this is normally done[1]. That is, a given amount of time, determined by T_P, after the read signal has been generated another signal is generated which allows the sense amplifier to produce an output if and only if the input at that time is of the proper magnitude. This requires that an AND function is performed in the sense amplifier. The strobing operation, then, logically ignores most of the noise during the read operation and all signals during the write operation. It should be noted, that if the sense amplifier is not internally strobed, it will probably produce an unwanted output during the write operation which will have to be inhibited by an AND operation elsewhere in the system.

Specifications for present day, commercially available bit planes show that the ratio of the one output voltage to the zero output voltage at time T_P is at least 3:1 and usually is more favorable. Such data is usually given for 64 x 64 bit planes containing 4096 cores. As the size of the bit plane is decreased, there will

be fewer and fewer noise producing cores, and the noise problem will diminish. The timing of the strobe signal will therefore become less critical as the memory size decreases.

5.2.3 Electronic Methods of Noise Reduction[2, 3]

There are two practical schemes that improve the discrimination between reading ones and zeros at the expense of longer read-write cycles and extra timing circuitry.

(1) The Post Write Disturb method applies a short duration half-read current pulse to every core in the memory after each write operation via the inhibit winding. Thus when a core is partially selected in the next read operation, its remanent flux will be very close to that of a disturbed one or an undisturbed zero, and the partial select current will produce only a very small change in remanence. The net result is that the difference in voltages between partially selected ones and zeros is about half what it is when write-disturbed ones and read-disturbed zeros are partially excited; also the noise produced by cores storing the same data will be practically identical. Noise cancellation is therefore more complete than when this method is not used and the partially selected cores have been previously disturbed in a random fashion.[3]

The post write disturb current pulse can be much shorter than the switching time of a core since it is only to produce small flux changes. However, in a low speed memory the inhibit current pulse generator (whose output is longer than T_S) might be used for the purpose.

(2) The Staggered Read Current scheme is based on the fact that most of the noise occurs during the rise of the half-read currents. Thus, the current in one direction, say the x direction, is caused to rise before the current in the other direction. The leading edges of the currents are staggered long enough in time so that all of the noise due to the cores in the x direction has died away before the y current is applied. The selected core will not switch until after the y current reaches its peak, and the information signal is not looked for until that time. Clearly the two currents must overlap for a time long enough for the selected core to switch.

In a square bit plane the method will give a 2:1 improvement in noise at the time the sense amplifier is strobed. If a rectangular bit plane is used and the long dimension is selected first, the improvement is still better; but it will be at the possible expense of more complex decoding logic.

This technique is often used with such large, high speed memories as the 8192 word, 1.5 μ sec. cycle-time memory in the DDP 116 computer.

In a low speed memory it seems possible that the two methods might be combined to give a good deal of noise reduction and freedom in the timing of the strobe pulse.

5.2.4 CCM Input Current Tolerances[2]

Worst case equations for the input currents may be easily written. First consider the half-read currents. Let the nominal value of the half-read current be symbolized by $I_{\frac{1}{2}R}$, and its tolerance by Δ_R expressed as a decimal, i.e., per cent divided by 100. I_{sm} is defined as the minimum current that will switch the core satisfactorally, and I_D is the maximum current which may be applied without destroying stored data.

To reset the addressed core it is necessary that

$$\left[2 I_{\frac{1}{2}R} \right]_{min} \geq I_{sm} \qquad (5.2.1)$$

where the min subscript implies the minimum value of the

variable. The minimum value of $I_{\frac{1}{2}R}$ is $I_{\frac{1}{2}R}(1 - \Delta_R)$, and the relationship may be rewritten as

$$2 I_{\frac{1}{2}R} (1 - \Delta_R) \geq I_{sm} \tag{5.2.2}$$

The maximum current through any partially selected core must not exceed the threshold current. Thus,

$$[I_{\frac{1}{2}R}]_{max} \leq I_D \tag{5.2.3}$$

which is rewritten as

$$I_{\frac{1}{2}R} (1 + \Delta_R) \leq I_D \tag{5.2.4}$$

Dividing (5.2.4) by (5.2.2) yields the requirement

$$\frac{I_D}{I_{sm}} \geq \frac{1}{2} \left(\frac{1 + \Delta_R}{1 - \Delta_R}\right) \tag{5.2.5}$$

or by rearranging

$$\Delta_R \leq \frac{I_D/I_{sm} - 1/2}{I_D/I_{sm} + 1/2} \tag{5.2.6}$$

The latter relation gives the allowable tolerance in the currents in terms of I_D/I_{sm}, and by choosing a minimum full read current for a given core, the maximum allowable tolerance can be determined by utilizing the equal sign. As would be expected Δ_R is zero when I_D/I_{sm} is 0.5, and it increases as I_D/I_M increases.

When Δ_R, I_{sm}, and I_D are known, then they may be substituted into (5.2.2) and (5.2.4) to determine $I_{\frac{1}{2}R}$.

For writing the interaction of the half-write currents $I_{\frac{1}{2}W}$ (having tolerance Δ_W) with the inhibit current I_I (having tolerance Δ_I) is considered.

To write a one at the addressed core the relationship is

$$[2\, I_{\frac{1}{2}W}]_{min} \geq I_{sm} \qquad (5.2.7)$$

to write a zero

$$[2\, I_{\frac{1}{2}W}]_{max} - I_{I_{min}} \leq I_D \qquad (5.2.8).$$

And the currents through unselected cores must be limited

$$[\, I_I \,]_{max} \leq I_D \tag{5.2.9}$$

$$[\, I_{\frac{1}{2}W} \,]_{max} \leq I_D \tag{5.2.10}$$

These are rewritten as

$$2\, I_{\frac{1}{2}W} (1 - \Delta_W) \geq I_{sm} \tag{5.2.11}$$

$$2\, I_{\frac{1}{2}W} (1 + \Delta_W) - I_I (1 - \Delta_I) \leq I_D \tag{5.2.12}$$

$$I_I (1 + \Delta_I) \leq I_D \tag{5.2.13}$$

$$I_{\frac{1}{2}W} (1 + \Delta_W) \leq I_D \tag{5.2.14}$$

The loosest tolerances will arise when the equal signs in (5.2.11) and (5.2.13) are taken so that

$$\frac{I_{\frac{1}{2}W}}{I_{sm}} = \frac{1}{2(1 - \Delta_W)} \tag{5.2.15}$$

$$\frac{I_I}{I_D} = \frac{1}{1 + \Delta_I} \tag{5.2.16}$$

Equations (5.2.12) and 5.2.16) may be combined to yield

$$I_{\frac{1}{2}W} \quad (1 + \Delta_W) \quad \leq \quad I_D \; - \; I_I \, \Delta_I \qquad (5.2.17)$$

thereby satisfying (5.2.14).

Finally (5.2.12), (5.2.15), and (5.2.16) are combined resulting in the requirement that

$$I_D/I_{sm} \quad \geq \quad \frac{1}{2}(1 + \Delta_I) \quad \left(\frac{1 + \Delta_W}{1 - \Delta_W}\right) \qquad (5.2.18)$$

In comparing this result with (5.2.5) it is seen that a higher I_D/I_{sm} is required for writing than for reading if all of the tolerances are the same. Conversely, for a given I_D/I_{sm} the read current drivers can have looser tolerances than the write current drivers. Nominal currents and I_{sm} can be made slightly different for the two cases. Oftentimes, however, the half read currents are produced to the same nominal value and tolerance as the half-write current to give operation on a symmetric hysteresis loop. However, as indicated in Section 4.3, UV_1 may vary considerably with temperature and full read current. With some cores it may be necessary to use tighter tolerances on the

read current than with other cores to obtain an output which is uniform enough to give reliable operation. Thus, the response characteristics of a core may demand a smaller Δ_R than that indicated by (5.2.6).

In Figure 5-7 the equalities of (5.2.5) and (5.2.18) for the special case $\Delta_I = \Delta_W$ are plotted to illustrate the difference. In Figure 5-8, Δ_I of (5.2.18) is plotted against Δ_W for several values of I_D/I_{sm} to illustrate the trade in tolerance between the information and addressing currents. In instances where there are many more drivers of one type than the other, a savings in cost will probably result if the tolerances are looser in the circuit which is most plentiful.

5.3 Practical L.S.M. Configurations

5.3.1 Typical Wiring and Noise

Ideally the decoding logic and gating in an LSM allows read current to flow through only the cores of the addressed registers; and therefore, there are no partially selected cores to produce noise. Also the read current is only in one dimension of the memory array, and it is no problem to eliminate mutual coupling between it and the sense lines which are everywhere

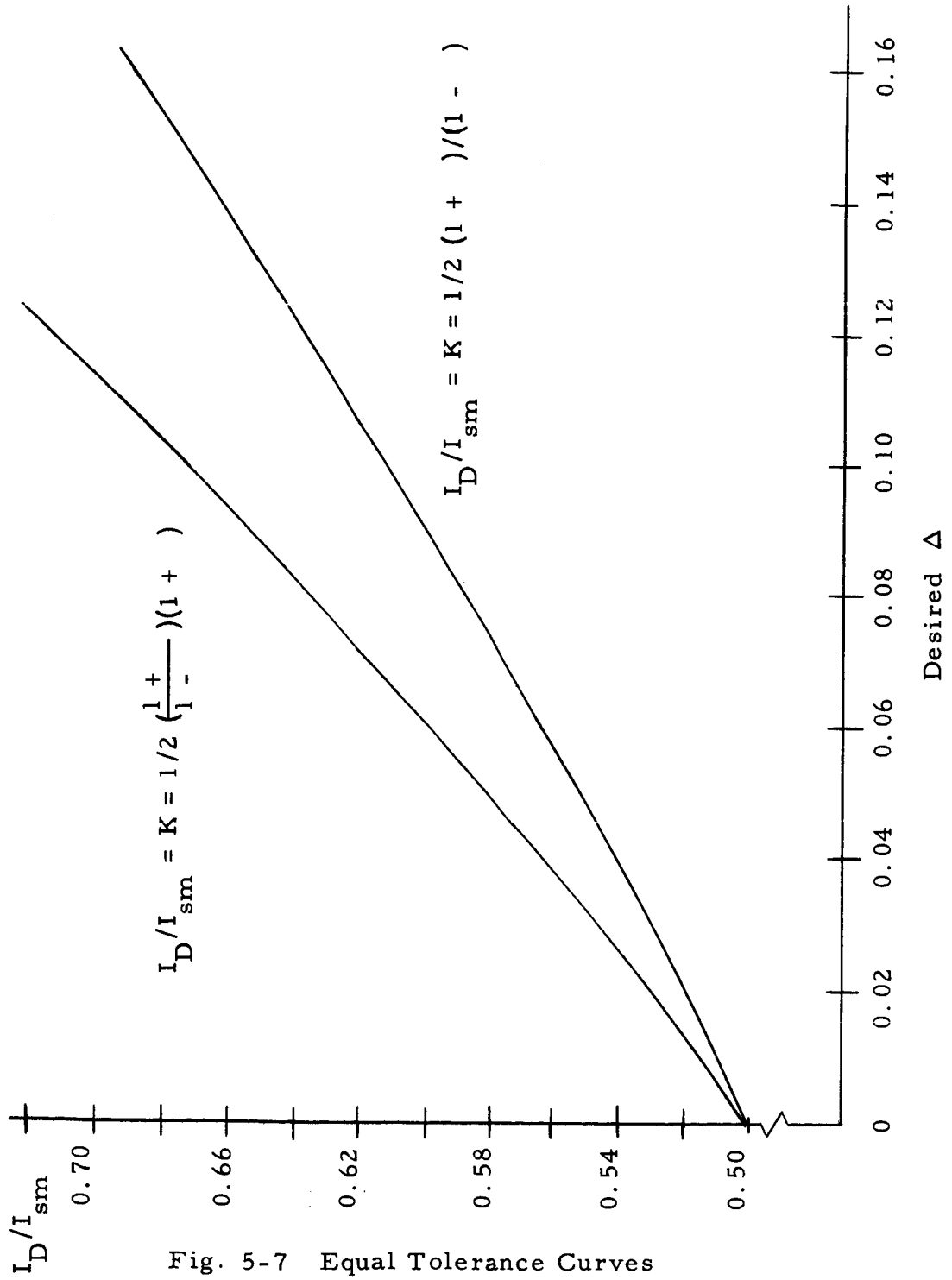


Fig. 5-7 Equal Tolerance Curves

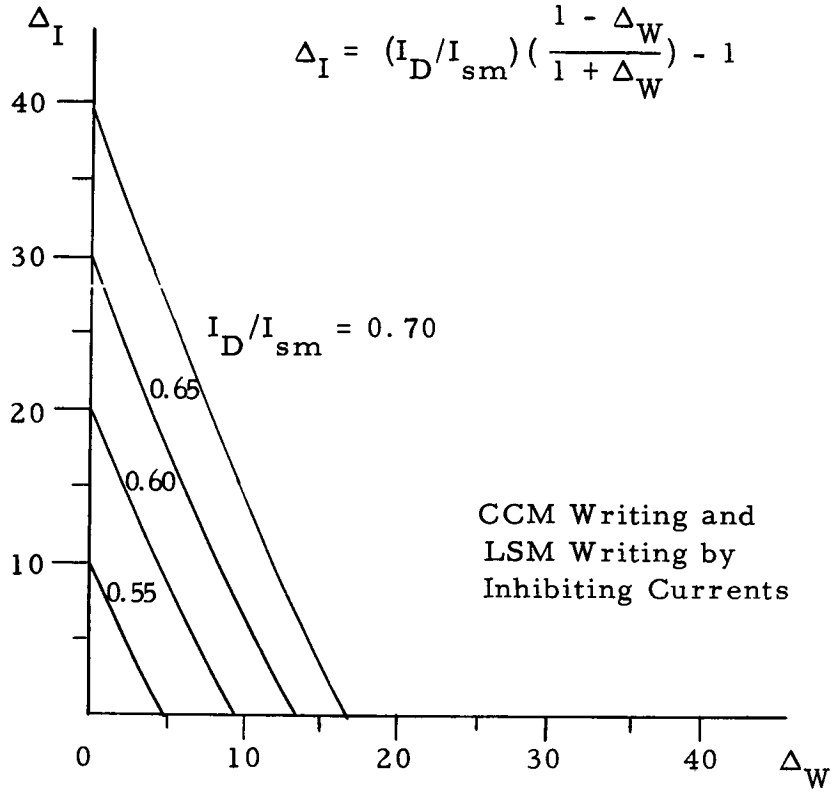


Fig. 5-8 Tolerance Trade Curves for CCM Writing

perpendicular to the read current. Thus, in comparison to the CCM there is virtually no noise problem, and a cancelling sense winding is usually not needed.

However, the decoding logic selects a switch of some sort, e.g., a transistor, and/or a current driver. Unselected elements of this type may allow small leakage currents to flow through unselected addresses resulting in very small voltages produced by unselected cores. For good operation, these leakage currents are kept very small, and the resultant noise will be much less than that produced by the partially selected cores in a CCM. (The same problem also occurs in the CCM but it automatically is taken care of by the cancelling sense winding). If the number of address is very large this noise may be significant enough to warrant the use of a cancelling sense winding.[5] For small memories it may be ignored and the memory wiring will be similar to that of Figure 3-12.

In Figure 3-12 a sense wire passes straight through all of the cores of its corresponding bit position, and then returns to the starting point. It is important that the return path of the wire is kept close to the length of wire which threads the cores in order to minimize any possible inductive cross talk between adjacent

sense wires. When a cancelling sense wire is needed, it may be readily formed by threading alternate cores in one direction through the plane and by threading the remaining cores on its return as illustrated in Figure 5-9. In either case it is necessary to form a twisted pair (or at least keep the two leads parallel and very close together) of the sense winding after it leaves the memory to minimize inductive cross talk with other circuitry.

It is observed from Figure 3-12 and Figure 5-9 that the sense wire is always parallel to the information current line, and in some instances it may be possible to use only one wire for both purposes as is shown in Figure 5-10. When separate wires are used, there is a good deal of capacitive coupling between the two which will cause large common mode voltage changes at the terminals of the sense winding as a result of current and voltage changes in the information current line.[6] When the two lines are combined into one, the sense amplifier will see directly the voltage changes that occur during the write operation; and because one end of the sense line will be at a fixed potential, this will not be a common-mode signal. If the two functions are combined on one wire, it will therefore be necessary to wait long enough (even in a very small memory) for all transients due to writing to die away

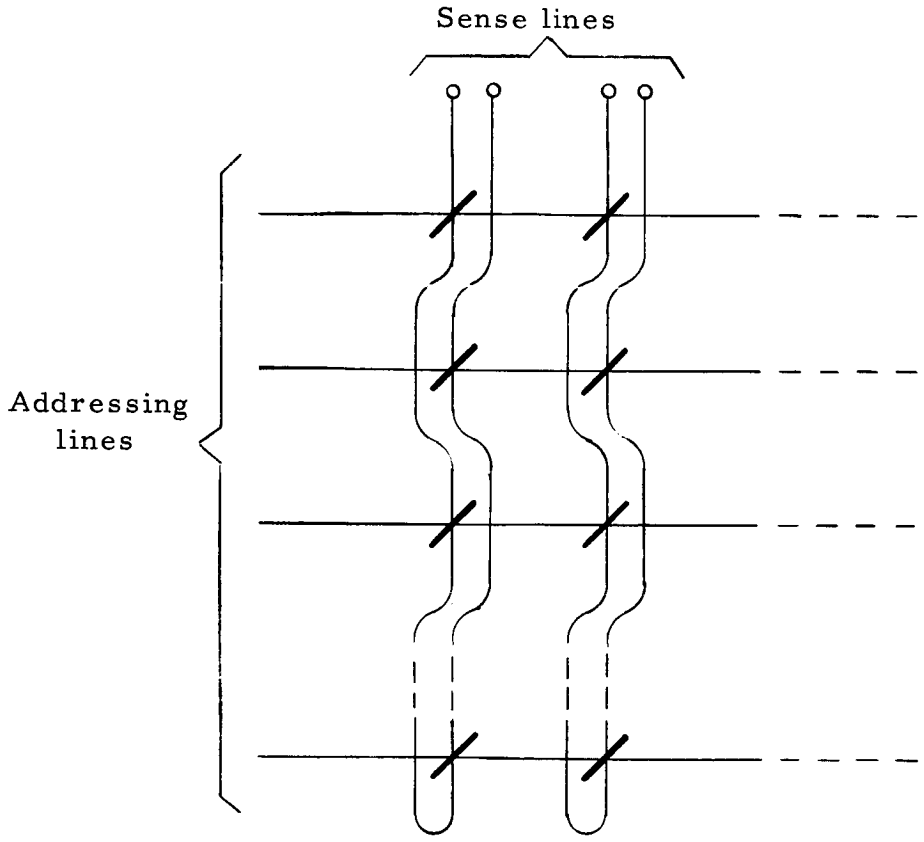


Fig. 5-9 Method of Threading Cancelling Sense Winding in an LSM
(Information current lines are not shown.)

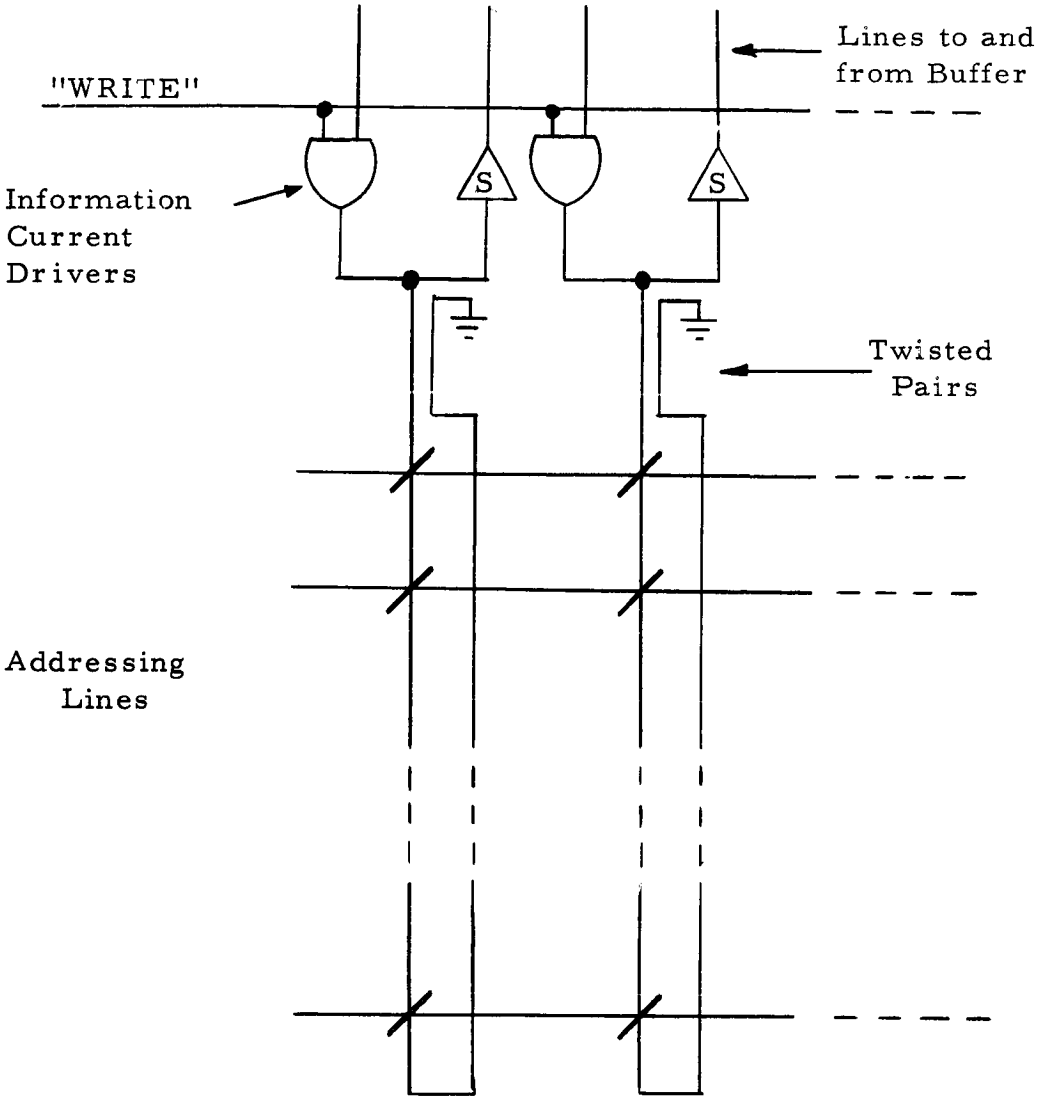


Fig. 5-10 Using Only One Wire per Buffer Bit for Both Information Current and Sensing

before reading. But because amplifiers may be readily built the reject common-mode signals (e.g., by use of a coupling transformer or by using a differential input stage), using separate wires will allow a much faster read/write cycle.

For larger LSM's it may be convenient to arrange the cores in three dimensions as in the CCM with bit planes[7]. If the bit planes are parallel to the xy plane, then the addressing currents will be in the z direction as indicated in Figure 5-11 which illustrates a three dimensional LSM

5.3.2 Writing Methods for the LSM[5]

The method of operating LSM described in Chapter 3, in which writing was done by augmenting currents, is a practical and workable means. However, in some cases other methods have proved more desirable, and three of these schemes are now described.

(1) Writing by Inhibiting Currents - In situations where addressing currents are produced by a device which readily forms positive and negative currents pulses of the same magnitude, the addressing currents for reading and writing are both of sufficient magnitude to switch a core. The AND operation in writing is

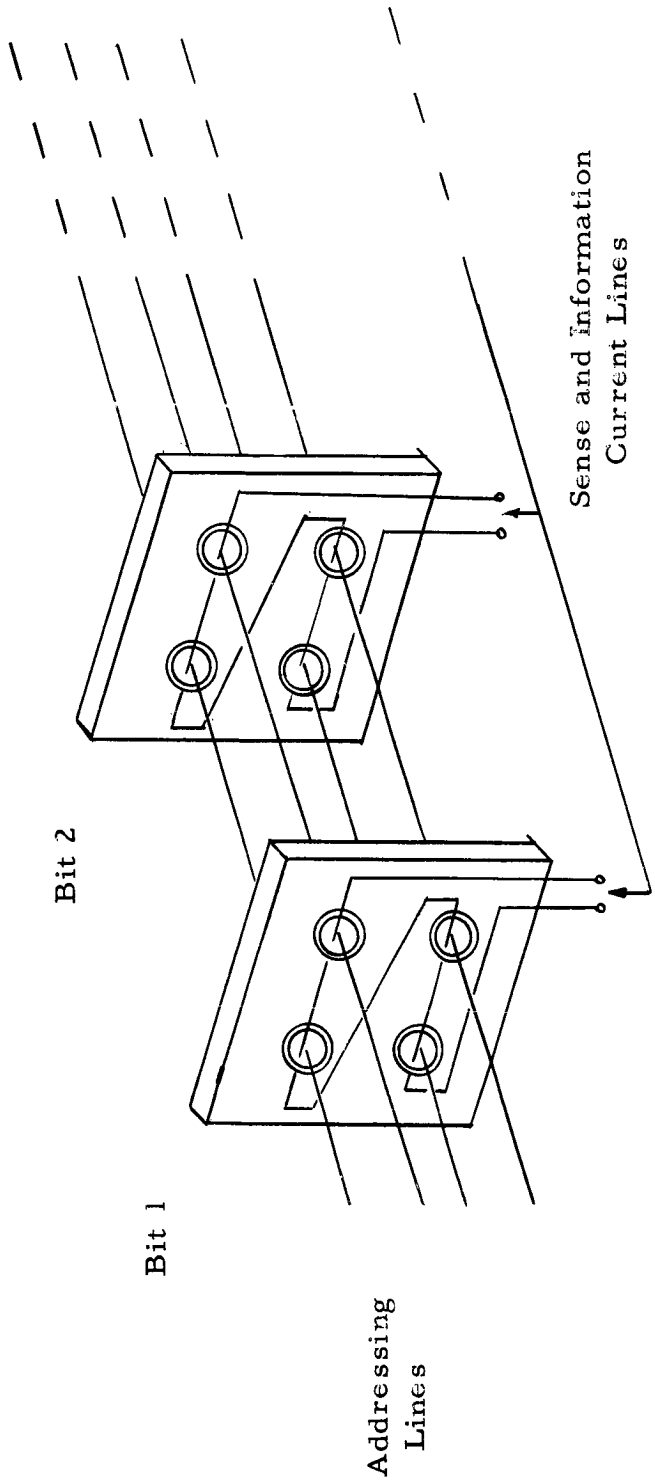


Fig. 5-11 A Method for Wiring an LSM in 3 Dimensions

therefore accomplished by the inhibit method. Thus, the addressing current for writing is $1_{S_{n+1}}^{W \cdot A_r}$, and the current in the information wire is $\frac{1}{2} R_{n+1}^{W \cdot \overline{B(s)}}$ in the notation of Chapter 2. The read current is $1 R_n^{R_d \cdot A_r}$. Unaddressed cores in the write operation receive the equivalent of half-read currents only, and when a one is read a UV_1 or a DV_1 may result. When a zero is read a DV_Z is produced if no half-read currents have been applied to the core or in the more usual case a signal somewhat less than DV_Z occurs since a prior half-read current would have driven the zero remnance flux back towards that of an undisturbed zero.

(2) Inhibit/Augment Systems - In these systems writing is accomplished by using an addressing current of $k_1 S_{n+1}^{W \cdot A_r}$, and the information current for writing a zero is $k_2 R_{n+1}^{W \cdot \overline{B(S)}}$; whereas to write a one the information current is $k_2 S_{n+1}^{W \cdot B(S)}$.

The constants must satisfy the relationships

$$k_1 + k_2 \geq 1 \qquad (5.3.1)$$

$$k_1 - k_2 \leq I_D/I_M \qquad (5.3.2)$$

$$k_2 \leq I_D/I_M \qquad (5.3.3)$$

and further constraints may be imposed upon them to achieve some special result. There are three interesting situations:

(a) The degree to which the state of any core in the memory is disturbed during writing is minimized if k_1 is chosen in the neighborhood of 2/3 and k_2 in the neighborhood of 1/3. A zero is then written with a current of 1/3 I_M, and the disturbing current to any unselected core is $\pm \frac{1}{3} I_M$. As a result discrimination in the output will be nearly between a UV_Z and a UV_1 which is an improvement over descrimination between a DV_Z and a UV_1.

(b) High writing speed is achieved if k_1 is chosen to be one and k_2 is 1/2. The current for writing a one will then be 1.5 times the minimal switching current, and the time required to do so (T_S) will be correspondingly small.[5]

(c) The constants may be selected to allow extremely loose current tolerances (approximately ± 20% for $I_D/I_M = 0.56$). This implies that the cost of the current drivers will be low; or that by using drivers with tighter tolerances, the memory will operate reliably over a wide temperature range.[7]

In the following section on current tolerances it is indicated how the nominal drive currents and their allowable

variations may be selected for each of the three cases.

It is observed that the advantages offered by these schemes are achieved at the cost of doubling the number of information-current drivers.

(3) Biased Cores[5, 6, 8]

Prior to every read-write cycle every core in the memory receives a bias current in the read direction of approximately one-half the necessary amount to reset a core, i.e., 1/2 R. This current is maintained throughout the entire cycle and is usually carried by a single wire which links all of the cores in a manner similar to that of the inhibit winding of Figure 3-15.

If the read current is $kR_n^{R_d \cdot A_r}$, then k need only be greater than 0.5; but it may be made much greater than this value to speed the reading process and/or give large peak values of output voltage.

Writing is accomplished by augmenting currents. The addressing current is $1\, S_{n+1}^{W \cdot A_r}$, and the information current is $1\, S_{n+1}^{W \cdot B(S)}$ to write a one, and zero to write a zero.

Because of the bias, the net current applied to an unaddressed core is essentially a half-read current (when there is zero information current) or a half-write current (when a one is written in the same bit position). When a zero is written, the net current through the addressed core is a half-write current. When a one is written, the net current is $3/2\ I_M$ producing rapid switching. Removing the bias after writing has the same effect as applying a post write disturb pulse; that is, the last excitation received by all cores is a half-read current, and remanent fluxes will be nearly those of disturbed ones or undisturbed zeros.

When the bias is applied prior to reading, every core in the memory is disturbed, and a great deal of noise is generated which may necessitate the use of a strobed sense amplifier. However, the bias may be left on continually during the time that the memory is being used, or in slow speed operation it may be turned on a long time before reading.

5.3.3 Current Tolerances for LSM's

The input current tolerance relationships for the four forms of LSM's just described are now derived. In all cases the following symbols are used for nominal drive current values.

I_R = read current

I_W = write addressing current

I_I = information current

I_B = bias current

Their tolerances are Δ_R, Δ_W, Δ_I, and Δ_B respectively, and all are expressed as decimals.

In general, the cores of an LSM are not operated on a symmetrical hysteresis loop since the read current will likely be made greater than the current used for writing ones.[5] I_{rm} will be used to denote the minimum acceptable value of current for reading, and I_{sm} will be used to signify the minimum acceptable current for writing ones.

In all of the four cases there is no upper limit on the total read current. Thus, for the first three systems the constraint is

$$I_{R_{min}} \geq I_{rm}$$

or

$$I_R (1 - \Delta_R) \geq I_{rm} \qquad (5.3.4)$$

And in the biased system

$$I_{R_{min}} + I_{B_{max}} \geq I_{rm}$$

or

$$I_R(1 - \Delta_R) \geq I_{rm} - I_B(1 - \Delta_B) \qquad (5.3.5)$$

A maximum limit on I_R may be imposed if it is desired to keep the switching time of the cores within a certain range which may be necessary if there is sufficient noise to warrant strobing the sense amplifiers with a good deal of precision. In determining I_{rm} from a core specification, recall that the smallest UV_1 and longest T_S occur at the lowest temperature.

The tolerances for writing in the four systems are now examined.

(1) Augmenting Currents - The worst case equations are:

(a) to write ones

$$I_{W_{min}} + I_{I_{min}} \geq I_{sm}$$

(b) to write zeros

$$I_{W_{max}} \leq I_D$$

(c) The upper limit on the information current is

$$I_{I_{max}} \leq I_D$$

These are rewritten in terms of the tolerances

$$I_W (1 - \Delta_W) + I_I (1 - \Delta_I) \geq I_{sm} \qquad (5.3.6)$$

$$I_W (1 + \Delta_W) \leq I_D \qquad (5.3.7)$$

$$I_I (1 + \Delta_I) \leq I_D \qquad (5.3.8)$$

Using the equal signs in the latter two relations will give the loosest tolerances. The values of I_I and I_W thereby obtained are substituted into (5.3.6) to give

$$\left[\frac{(1 - \Delta_W)}{(1 + \Delta_W)} + \frac{(1 - \Delta_I)}{(1 + \Delta_I)}\right] I_D/I_{sm} \geq 1 \qquad (5.3.9)$$

This relationship must be satisfied in the memory design. Fig. 5-12 is a plot of Δ_I vs Δ_W for several values of I_D/I_{sm}. Observe that if the tolerances are made equal,

$$\Delta_I = \Delta_W = \Delta \qquad (5.3.10)$$

"AND" BY TWO AUGMENTING CURRENTS

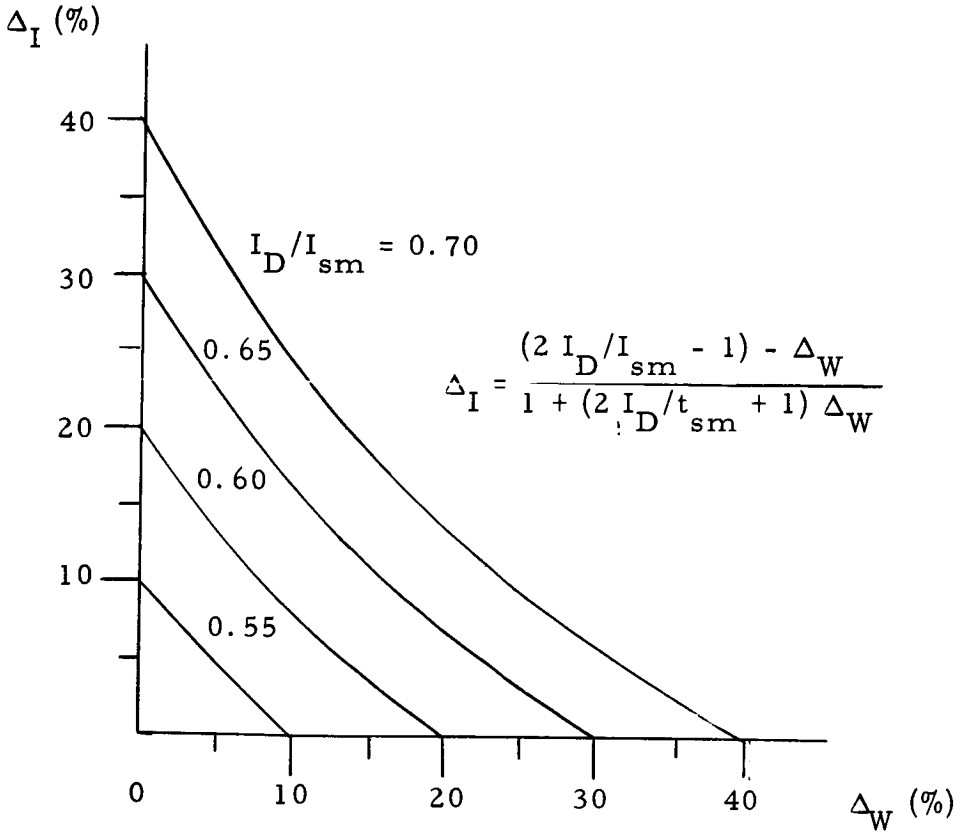


Fig. 5-12 Tolerance Trade for Writing by Augmenting Currents in an LSM

then the relationship

$$\frac{I_D}{I_{sm}} \geq \frac{1}{2}\left(\frac{1+\Delta}{1-\Delta}\right) \tag{5.3.11}$$

results. This is the same as Equation (5.2.5) for the half-read current tolerances of a CCM.

(2) Inhibiting Currents: The worst case equations are written directly in terms of the tolerances:

To write ones

$$I_W\,(1-\Delta_W) \geq I_{sm} \tag{5.3.12}$$

To write zeros

$$I_W\,(1+\Delta_W) - I_I(1-\Delta_I) \leq I_D \tag{5.3.13}$$

and to limit the information current

$$I_I\,(1+\Delta_I) \leq I_D \tag{5.3.14}$$

Taking the equal signs in (5.3.12) and (5.3.14) solving for I_W and I_I, and substituting into (5.3.12) results in the constraint.

$$I_D/I_{sm} \geq \frac{1}{2}(1+\Delta_I)\left(\frac{1-\Delta_W}{1+\Delta_W}\right) \tag{5.3.14}$$

which is the same as equation (5.2.18) derived for writing in a CCM, and it is plotted in Fig. 5-8. Notice that the tolerances in this case are tighter than those for writing by augmenting currents.

(3) Inhibit/Augment System

The worst case equations in terms of the tolerances are:

To write ones:

$$I_W(1 - \Delta_W) + I_I (1 - \Delta_I) \geq I_{sm} \qquad (5.3.15)$$

To write zeros

$$I_W (1 + \Delta_W) - I_I (1 - \Delta_I) \leq I_D \qquad (5.3.16)$$

and to limit the information current

$$I_I (1 + \Delta_I) \leq I_D \qquad (5.3.17)$$

Using the equal signs, equations (5.3.18) and (5.3.16) are combined to give

$$I_W/I_{sm} = \frac{1}{2}(1 + I_D/I_{sm}) \qquad (5.3.19)$$

From which the nominal value of I_W which gives the loosest tolerances for a given I_{sm} may be calculated.

Again using the equal signs, Equation (5.3.17) is substituted into the right-hand side of (5.3.16), and the ratio of nominal drive currents to give the greatest tolerances results.

$$I_I/I_W = \frac{1 + \Delta_W}{2} \qquad (5.3.20)$$

The relationship between the tolerances and I_D/I_{sm} is then found from (5.3.17) to be

$$(1 + \Delta_W)(1 + \Delta_I) \leq \frac{4(I_D/I_{sm})}{1 + (I_D/I_{sm}} \qquad (5.3.21)$$

which holds only when (5.3.19) and (5.3.20) are adhered to.

Δ_I is plotted against Δ_W for the equality of (5.3.21) in Fig. 5-13, and Fig. 5-14 is a plot of I_D/I_M for the special case when $\Delta_I = \Delta_W = \Delta$. Observe that when both tolerances are zero, I_D/I_{sm} may be as low as 1/3; whereas, in all previously discussed cases I_D/I_{sm} could only be as low as 1/2 for this limiting situation. When the tolerances are $\pm$ 15% or less, a value of I_D/I_{sm} greater than 1/2 will give reliable operation. It is this greater freedom in tolerances which makes possible the three situations previously described for this writing method. Properly interpreting I_D/I_{sm}

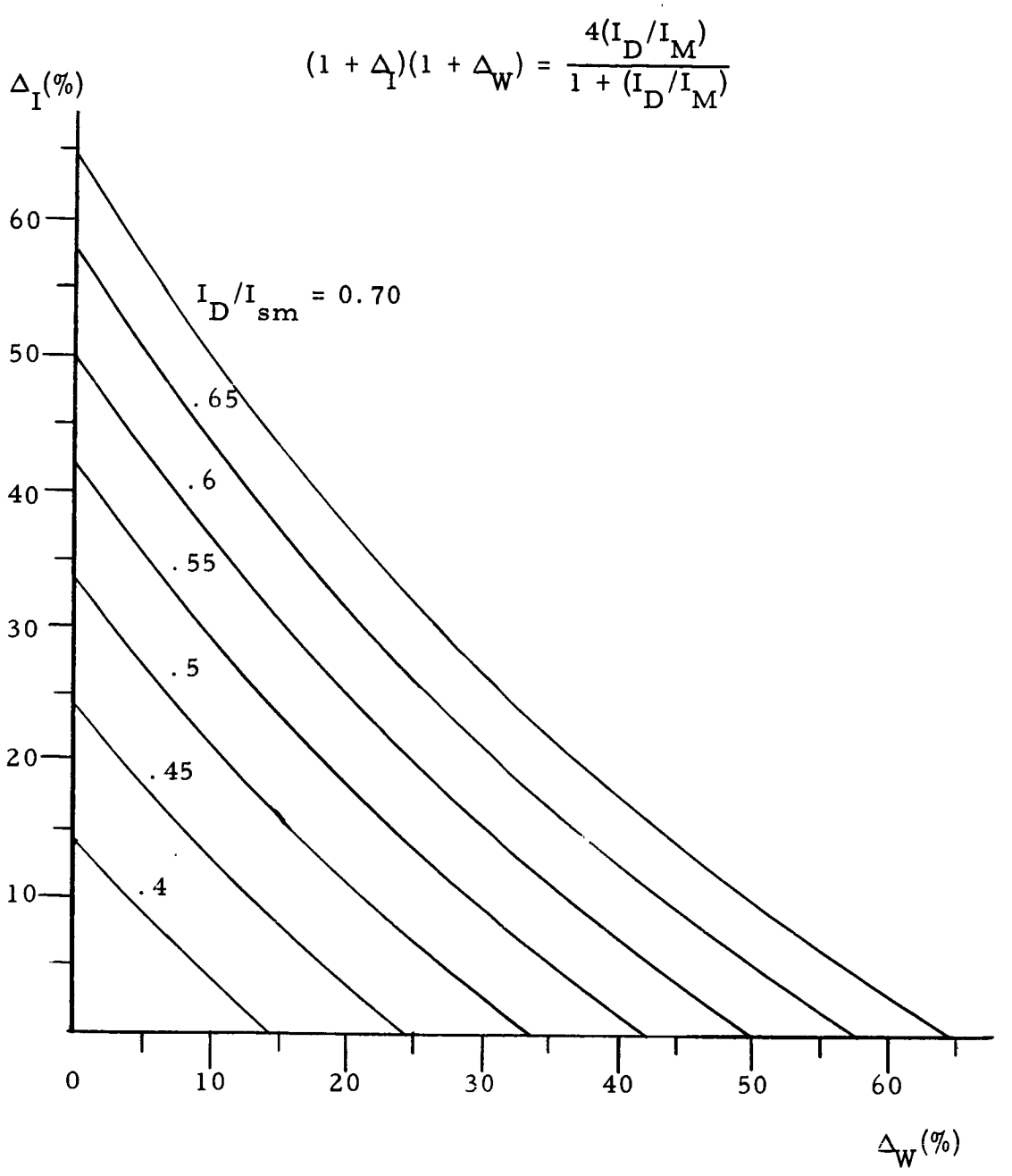


Fig. 5-13 Tolerance Trade in Writing by Inhibit/Augment Method in LSM

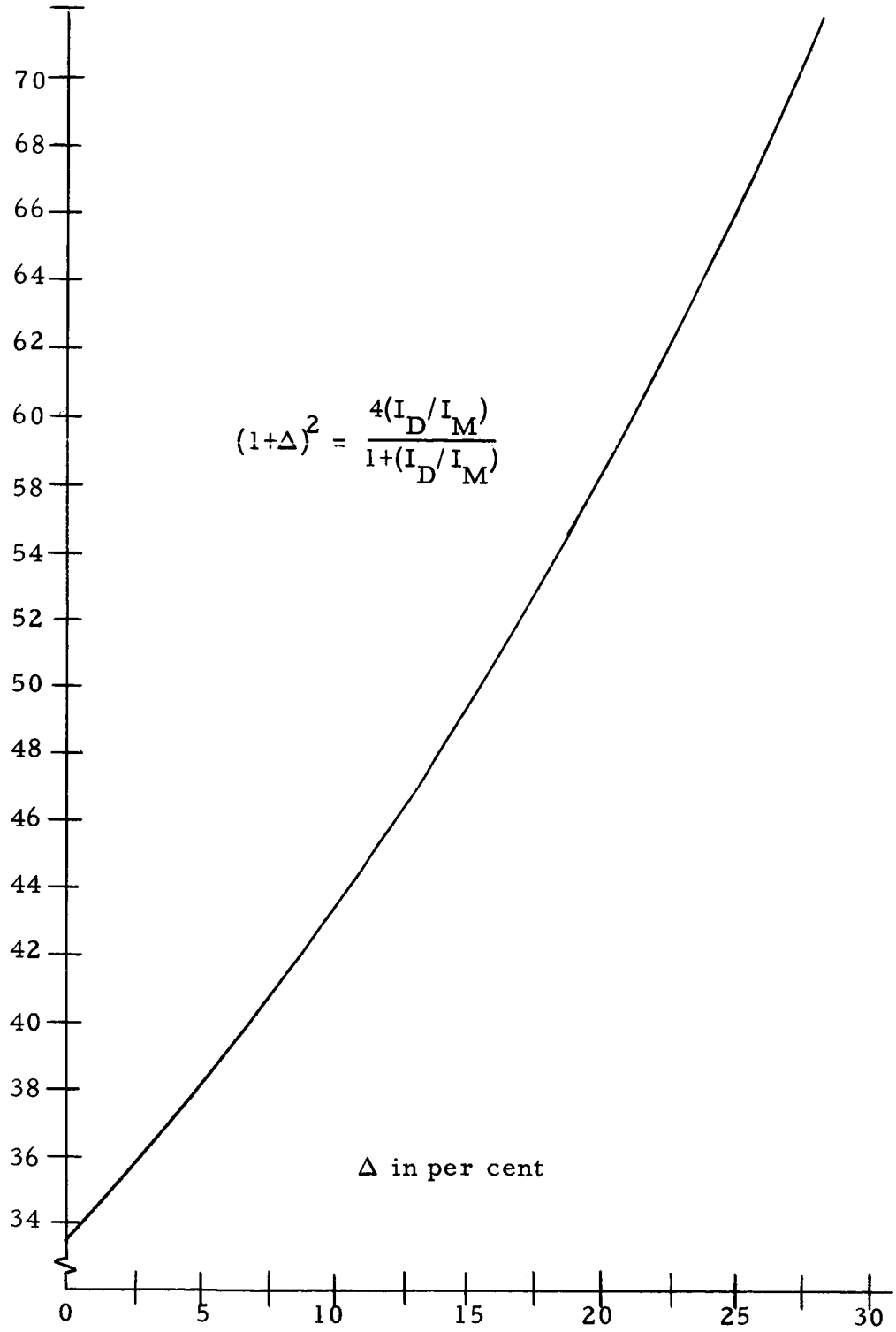


Fig. 5-14 Equal Tolerance curve for Inhibit/Augment System

will allow the relationships just derived to be used for each case. These are now examined in turn.

(a) Minimum Disturbance: Here I_D/I_{sm} is not determined from the core specifications, but it is defined so that the disturbing currents will be as small as practically possible. This is the same as defining a new threshold current for the core which is considerably less than the actual threshold. The value of I_D/I_{sm} is therefore determined by the desired current tolerances, and it is chosen from the plots to be as small as possible. Then I_W/I_{sm} and I_I/I_W are calculated from (5.3.20) and (5.3.21). A core with a suitable UV_1 is selected, and a minimum value of switching current (e.g., the value to which the core was tested) is used for I_{sm} to determine I_W and I_I. The amplitude of the read current is of course independent of these calculations, and it is selected to give a convenient output.

(b) High Writing Speed: In this case I_D/I_{sm} may be taken from the core specification sheets to correspond to an I_{sm} which gives a short switching time. These values are then used to calculate I_W and I_I. Manufacturer's data generally is not extended beyond currents for which I_D/I_M is less than 0.5, but if need be it is possible to extrapolate beyond this point since the behavior of the variables is nearly linear with drive current.

(c) Loosest Tolerances or Wide Temperature Range:

The loosest tolerances occur when I_{sm} is chosen to be near the minimum switching current and the corresponding high value of I_D/I_{sm} from the core specification is used. If I_D/I_{sm} is 0.65, for example, then the tolerances on the currents from Fig. 5-14 are ± 25%. If this value if I_{sm} is selected at the low temperature extreme at which the memory is to operate and the current drivers have tighter tolerances, the memory will operate reliably at higher temperatures with the upper limit being the temperature at which I_D/I_{sm} for the selected I_{sm} satisfies the equality of Equation (5.3.21). For example, if the currents have tolerances of ± 7%, I_D/I_{sm} may be as low as 0.40. I_{sm} is chosen so that I_D/I_{sm} is greater than this value at the high temperature extreme. This will correspond to a fairly high value of current at which ones may be satisfactorily written at a much lower temperature.

(4) Biased Core System

The worst-case equations are:

For the bias current

$$I_B (1 + \Delta_B) \leq I_D \qquad (5.3.22)$$

To write ones

$$-I_B(1 + \Delta_B) + I_W(1 - \Delta_W) + I_I(1 - \Delta_I) \geq I_{sm} \qquad (5.3.23)$$

To write zeros

$$-I_B(1 - \Delta_B) + I_W(1 + \Delta_W) \leq I_D \qquad (5.3.24)$$

and to limit the information current

$$-I_B(1 - \Delta_B) + I_I(1 + \Delta_I) \leq I_D \qquad (5.3.25)$$

Observe that the effect of the bias current is to move the origin of the hysteresis loop to $I_B(1 \pm \Delta_B)$.

Equation (5.3.22) determines the bias current

$$I_B \leq \frac{I_D}{1 + \Delta_B} = \frac{(I_D/I_{sm})\, I_{sm}}{1 + \Delta_B} \qquad (5.3.26)$$

Choosing I_B to be as large as possible will allow the greatest net full write current and, therefore, the fastest writing speed. Hence, the equality of (5.3.26) would normally be used. Since only one current source is required for I_B, Δ_B may be readily made small (less than 5%) at not too great an extra expense for the entire memory.

Equation (5.3.26) is substituted into (5.3.23) and (5.3.25) (using the equal signs) to arrive at the following relations for determining the nominal values of the drive currents.

$$I_W = \frac{2(I_D/I_{sm})\, I_D}{(1+\Delta_B)(1+\Delta_W)} \qquad (5.3.27)$$

$$I_I = \frac{2(I_D/I_{sm})\, I_D}{(1+\Delta_B)(1+\Delta_W)} \qquad (5.3.28)$$

Substituting these results into (5.3.24) gives the relationship between the tolerances and I_D/I_{sm}

$$\left(\frac{1-\Delta_W}{1+\Delta_W}\right) + \left(\frac{1-\Delta_I}{1+\Delta_I}\right) \quad \frac{2(I_D/I_{sm})}{(1+\Delta_B)(1+I_D/I_{sm})} \geq 1 \qquad (5.3.29)$$

Note that if $(I_D/I_{sm})'$ is defined as

$$(I_D/I_{sm})' = \frac{\text{(maximum allowable current for not switching)}}{\text{(minimum allowable current for switching)}}, \qquad (5.3.30)$$

where the currents are applied after the bias has been established, and calculated as follows

$$(I_D/I_{sm})' = \frac{I_B(1 - \Delta_B) + I_D}{I_B(1 + \Delta_B) + I_{sm}} = \frac{2(I_D/I_{sm})}{(1+\Delta_B)(1 + I_D/I_{sm})} , \quad (5.3.31)$$

it is seen that the requirement of (5.3.29) may be written as

$$\left[\left(\frac{1 - \Delta_W}{1 + \Delta_W}\right) + \left(\frac{1 - \Delta_I}{1 + \Delta_I}\right) \right] (I_D/I_{sm})' \geq 1 \quad (5.3.32)$$

This is the same as the relationship (5.3.9) for the writing by augmenting currents system, and the plots of Fig. 5-7 and Fig. 5-12 may be accordingly used.

Since I_D/I_{sm} and Δ_B are both less than one and positive, it can be determined from (5.3.31) that

$$(I_D/I_{sm})' > I_D/I_{sm} \quad (5.3.33)$$

which shows that the bias current effectively improves the threshold of the core. The implication is, of course, that the current tolerances can be loosened or a wider temperature range is more feasible than with the augmenting current scheme first described.

5.4 Comparison of the CCM and the LSM

As stated before, the biggest advantage of the CCM over the LSM is in the simpler decoding logic. On the other hand the L.S.M. offers the following advantages which tend to offset the extra cost of the decoding logic.

(1) Because the sense outputs are always of the same polarity and the noise is small in comparison to a CCM the sense amplifier will be less costly for the LSM.

(2) The read current tolerances are very loose, and the write current tolerances are generally looser than those of a CCM (exception - writing by the inhibit current method gives the same tolerances as the CCM). This implies that although more current pulse generators will probably be required by the LSM, (Chapter 7 shows how the number of current drivers may be reduced), the cost of each will be less.

(3) The LSM offers higher speed capabilities.

(4) The wiring of the cores for an LSM is simpler than for a CCM. Hence, the cost of stringing the cores for the LSM will be considerably less.

5.5 Special Purpose Memories

The memories described to this point are general purpose in nature; each address is as readily accessible as any other, and new data may be written at any address after reading. It is to be expected that system requirements will specify that some of the features of these memories are not needed and in many instances savings in the amount of peripheral equipment (sense amplifiers, current drivers, etc.,) may result by designing a memory especially for the purpose at hand. Three examples of special-purpose memories are now presented to indicate to the designer what can be done.

5.5.1 Permanent Data Storage

A core memory may be readily constructed which will permanently store data for the life of the system. The data is inserted at each address in the construction process by physically ensuring that upon a full select excitation a core will change states and induce a UV_1 or DV_1 voltage on the appropriate sense winding everywhere a one is to be stored and that a core will not induce such a voltage (except perhaps for a small noise voltage) where a zero is to be stored. The memory is operated by resetting each core at the selected address to read the stored word. After

reading, the system is readied for the next read operation by setting each core at the address or in the entire memory by a full write current.

In a conventional memory array (a CCM or LSM) this may be accomplished in several ways including [9]:

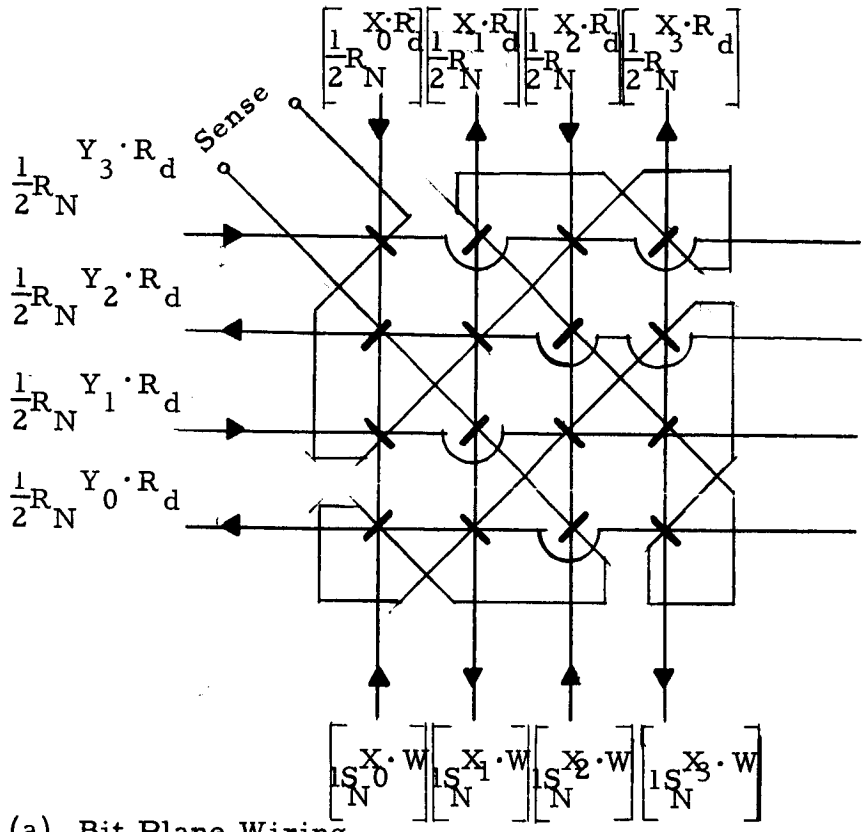
(1) Omitting the core wherever a zero is to be stored.

(2) by passing zero-storing cores with one or more drive windings.

(3) by passing zero-storing cores with the sense winding.

Observe that using these techniques in a CCM can result in a worsening of the noise problem because the number of non-cancelling, partially selected cores will increase. One way to avoid this is by inserting zeros by bypassing cores with drive wires in one dimension only, and staggering the half-read currents so that the current in the dimension which threads all cores is applied last. Fig. 5-15 illustrates this.

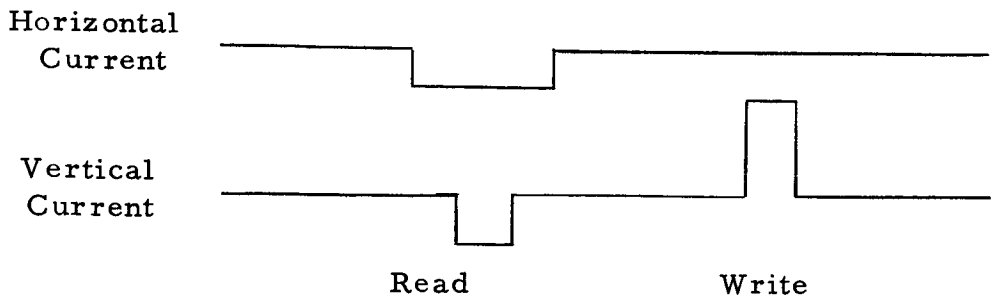
Permanent data storage memories may also be constructed using only one core for each word to be stored, or



(a) Bit Plane Wiring

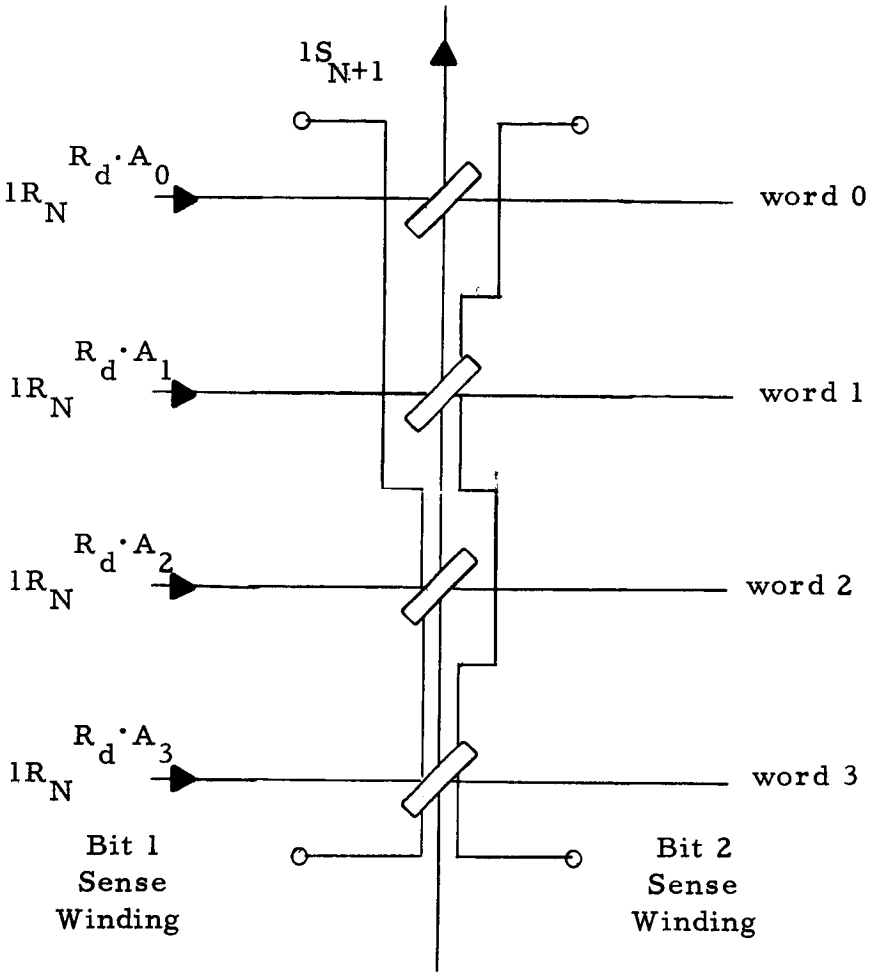
1	0	1	0
1	1	0	0
1	0	1	1
1	1	0	1

(b) Stored Data



(c) Current Timing

Fig. 5-15 Example of Permanent Data Storing CCM Bit Plane

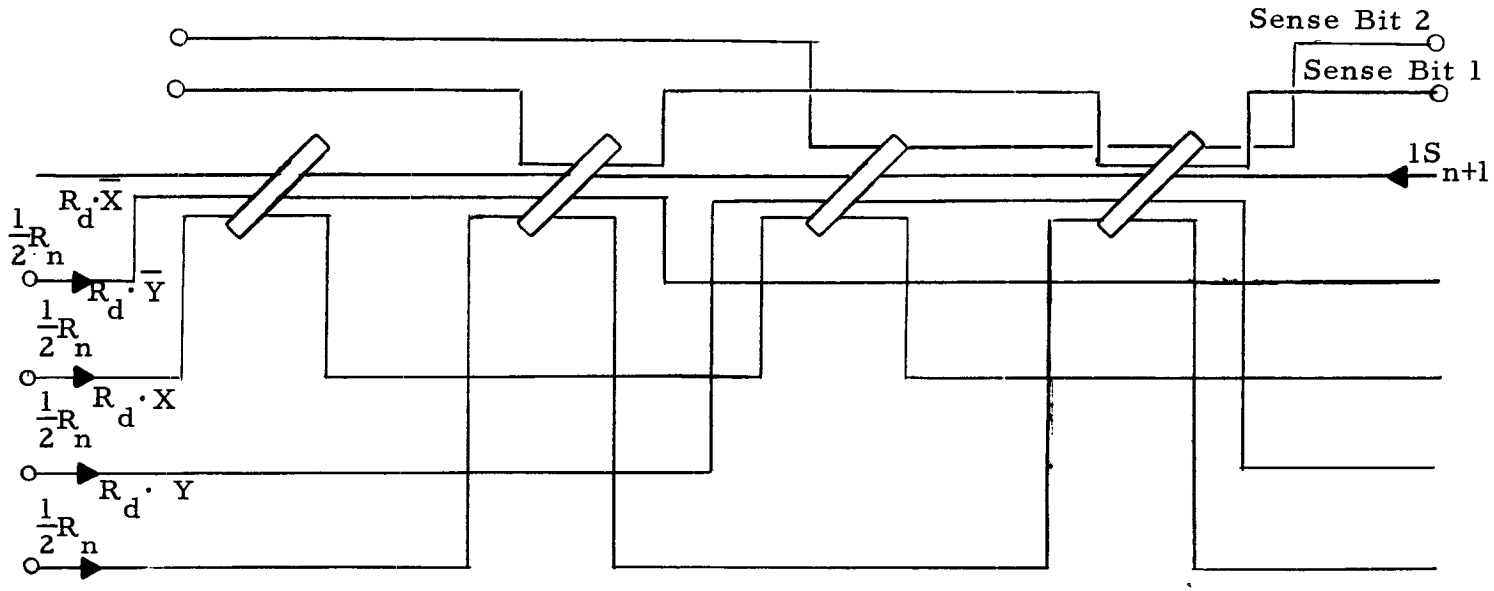


		OUTPUT	
Word	Address	Bit 1	Bit 2
0	A_0	0	0
1	A_1	0	1
2	A_2	1	0
3	A_3	1	1

Fig. 5-16 One Core Per Word Permanent Data Storage.

only one core for each bit position of the stored words. That is, permanent storage for m words of n bits each may be achieved using only m or n cores[9, 10, 11]. The methods are indicated in the following examples.

Fig. 5-16 illustrates a four-word, two-bit memory using one core for each word. There is a sense winding corresponding to each bit, and a sense winding links a core only when the corresponding bit of the word at the address of the core is to be a one. All cores are initially in the one state; and when a word is read at time n, the addressing current, $1R_n^{R_d \cdot A_i}$, resets the core at the desired address A_i inducing voltages on the sense windings threading that core. After the read operation all cores receive a set current $1S_{n+1}$ which initializes the system for the next read input. Notice that the threshold property of the square loop core has not been used, and it is not necessary to use square loop cores for this type of system. However, if square loop cores are used, the threshold may be taken advantage of using coincident-currents to select the proper core and thereby reduce the necessary decoding logic.[9, 10, 11] One possible arrangement is shown in Fig. 5-17.



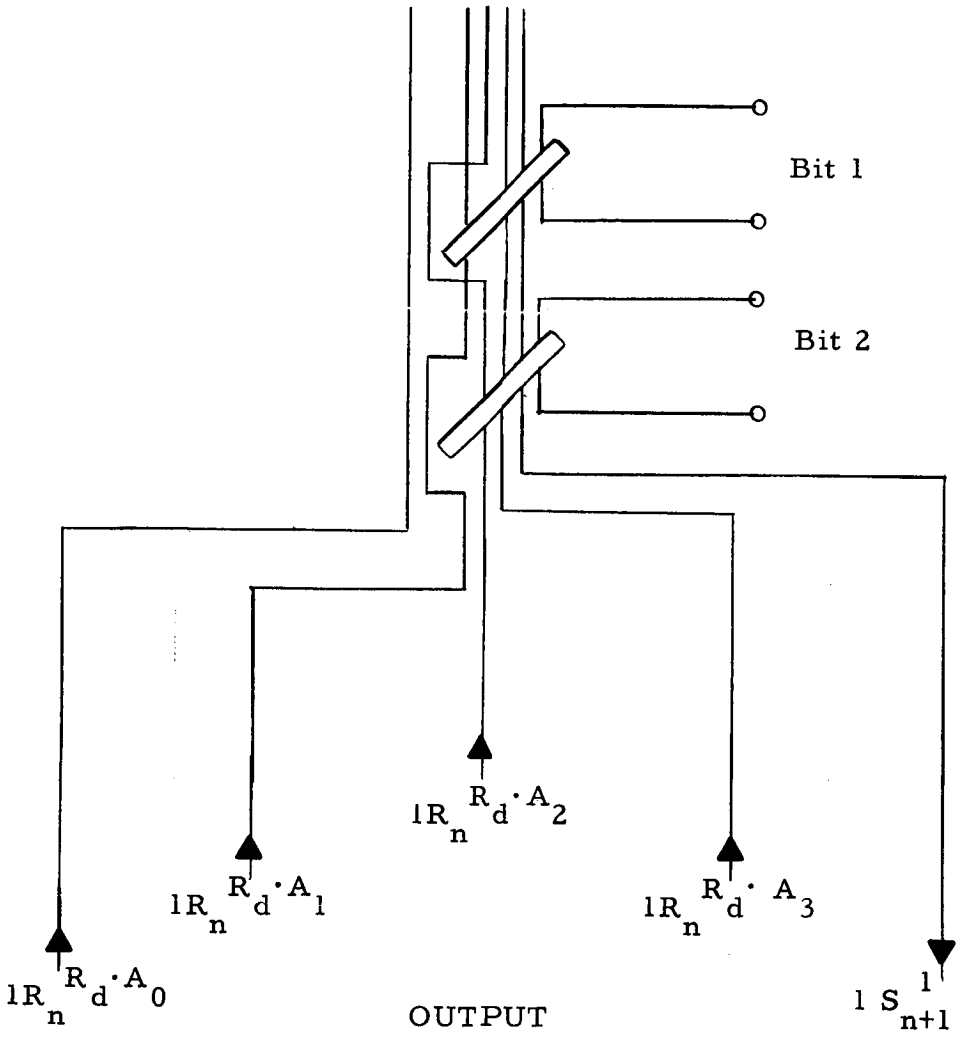
ADDRESS	Bit 2	Bit 1
$A_0 = \bar{X} \cdot \bar{Y}$	0	0
$A_1 = \bar{X} \cdot Y$	0	1
$A_2 = X \cdot Y$	1	0
$A_3 = XY$	1	1

Fig. 5-17: One Core Per Word Storage Using Coincident Current Selection.

Fig. 5-18 illustrates the principle involved using one core per output bit. The memory shown provides the same outputs for the same logical inputs as does the one in Fig. 5-16. A sense winding threads each of the two cores. Four drive wires, each corresponding to one of the four words, pass through only those cores where a one is to be present in the output. As in the previous example, all cores are initially in the one state. The word at address A_i is read by applying $1R_n R_d \cdot A_i$ to the proper drive wire. After reading $1S_{n+1}$ is applied to both cores to reinitialize the memory. For memories of any appreciable size both the one core per word and one core per bit 'ideas' pose difficult wiring problems. It will probably be necessary to use large sized switch cores in order to fit all of the wires through. This is not too desirable, since the large cores will require much larger input currents than the small memory cores.

5.5.2 Data Delaying and Data Rate Changing Memory

Bursts of parallel digital data can be delayed, and the rate of information flow in the bursts changed by a magnetic core memory. The memory must have sufficient storage capacity for all of the words in a burst of data. The controlling logic is designed to write each new data word at a new address; thus, the



OUTPUT

ADDRESS	Bit 2	Bit 1
A_0	0	0
A_1	0	1
A_2	1	0
A_3	1	1

Fig. 5-18 One Core Per Output Bit Permanent Data Storage

address register may be a binary counter which is incremented one count after each such operation. The data is read out at a later time (but before the next burst of data) at a convenient rate of sequencing through all of the memory addresses and reading at each address.

Clearly the usual read-write cycle need not be adhered to, and faster operation times with less expenditure of energy will result if it is not. In particular assume that the memory is initially cleared before a burst of new data. Each information word may be written at each address without first having to read, i.e., reset, the storage register at that address. When the data is read from the memory, no write operation will follow any read operation; and the memory will be left cleared for the next burst. In effect the entire memory operates in a single write-read cycle.

A possible use for such a memory would be to transfer data from magnetic tape to punched tape and vise versa since magnetic tape normally operates at a higher speed than does punched tape.

5.5.3 LSM With Serial Data Output

Fig. 5-19 shows four word, four bit LSM which gives serial data output. The addressing current in the horizontal direction is a half-read current, and half-read currents are applied sequentially to the verticle lines so that the cores of the addressed storage register receive full-read currents at different times sequenced from left to right. The stored word is thus transferred serially to the single cancelling sense winding, which links every core of the memory.

The writing technique shown is the usual augment method, but other methods may be used, and a serial method of writing can also be readily devised.

5.5.4 General Comments

The three examples of special purpose memories given may be combined and extended to form other systems; e.g., a permanent data storage with serial output.

It should be noted that the results of all of any of these could be obtained by suitably controlling a conventional CCM or LSM. For example, serial data output could be achieved by reading in parallel into a buffer register designed to shift the word

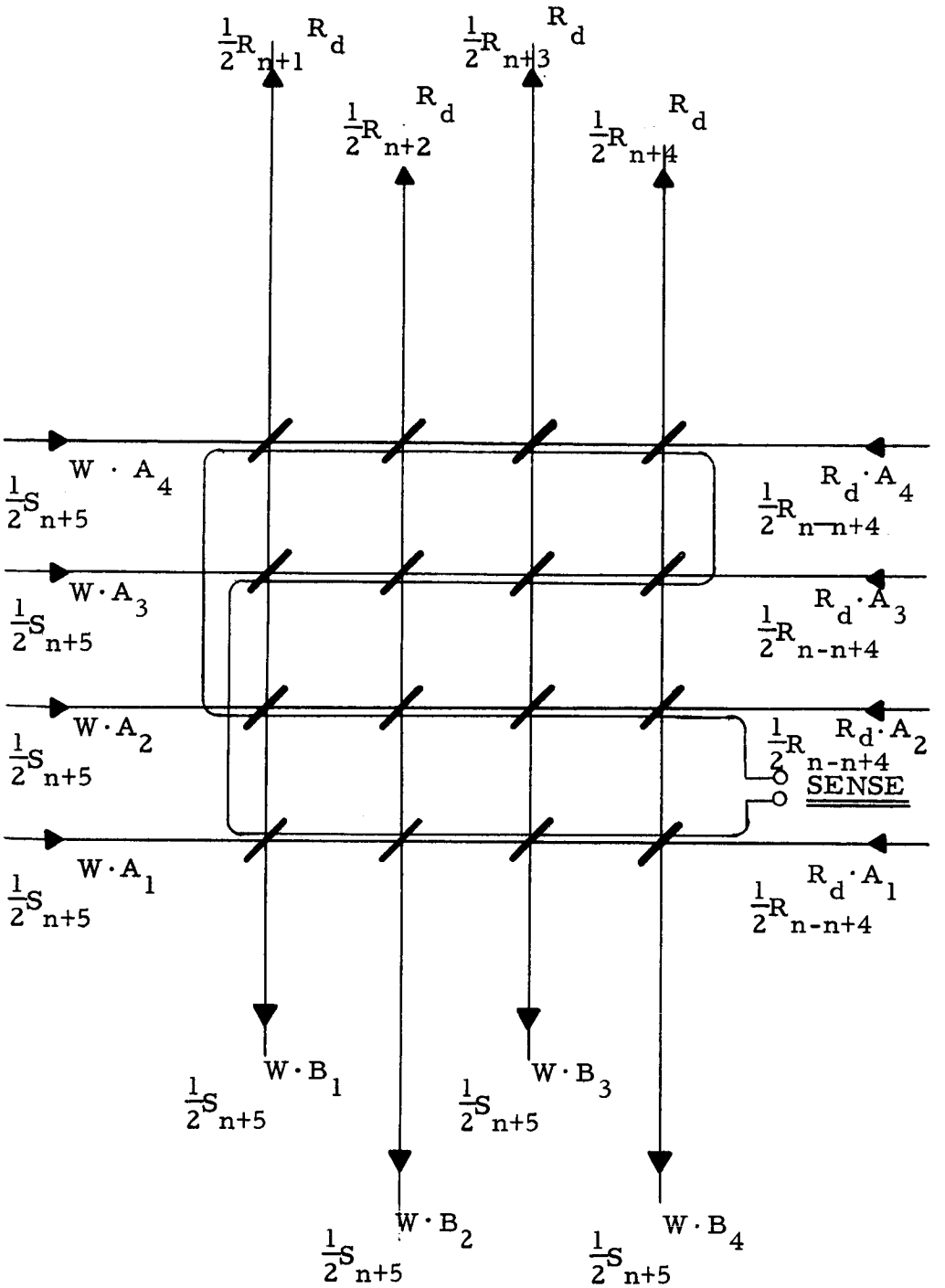


Fig. 5-19 Serial Output Technique

out to the logic system serially.

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CHAPTER 6

CURRENT DRIVERS

6.1 Design Considerations

Current drivers are used to convert signals generated by the logic system to the current pulses required to operate the memory. Thus, the input to a current driver is normally a logic signal whose characteristics - voltage swing, rise time, etc., - should be considered.

Usually the desired shape of the current pulse (the output of the driver) is nearly square or trapazoidal as shown in Fig. 4-3a. Important considerations as to the size and shape of the current pulse are:

(1) The amplitude and its allowable tolerance. This information may be obtained from the worst case input current equations for the memory configuration and the characteristics of the core chosen for use.

(2) The required rise time which is a function of the core characteristics, the purpose of the current, and the speed at which the memory is to operate. For a read current it is usually necessary to use a rise time close to the one suggested by the core manufacturer for good discrimination in the memory output. For

write currents the manner in which the core switches is not critical; and therefore, the rise time is critical only where high speeds (which indicates that a short rise time be used to switch the cores as rapidly as possible) are required. Where high writing speeds are not involved, the rise time of the write current may be much longer than the manufacturer's specified rise time.

(3) The Time duration of the pulse must be long enough to allow the core to switch. The maximum switching time at the value of drive current being used is therefore the lower limit on the pulse width. In cases where the coincidence of two or more currents is used, the currents must be coincident for a time greater than the core's switching time; and to ensure that they will be coincident for a long enough time it is usually necessary that the time durations of the individual pulses be longer than the core's switching time. Also in low speed writing where a long rise time is used the time duration should be made quite long since the core will require a longer time to switch than is indicated by the specifications.

(4) The fall time of the pulse is not critical in a low speed memory. At higher speeds it would be desirable to use a fall time as short as possible to give minimal time per operation. It should, however, be observed that a very short fall time might

(c) The voltage induced by the cores on the drive wire which do not switch. Like (b) above, the peak of this voltage occurs during the rise of the current, and the peak value increases with decreasing rise time.

(d) The voltage induced by all cores on the drive wire that do switch. For short rise times the peak of this component occurs after the current rise.

Fig. 6-1 illustrates the four components developed across a core line and their sum (which is the total voltage) which result from a typical, trapazoidal drive current. In a small memory, the drive wires may be kept short and their impedances small so that the first two components listed will become negligible.

In many memories a system of diodes, gates, and switches is used to route the current pulse to one of several lines of cores as a part of the decoding logic[3], and the voltage drops which occur across these elements must also be taken into consideration. This is neglected in the remainder of this chapter but considered when these gating systems are discussed in Chapter 8.

produce sufficient fly back voltage to adversely effect the current driver.

Other considerations are:

(5) The repetition rate, or how often the pulse must be formed, will effect the power ratings of the circuit components of the driver. The higher the repetition rate the greater the power ratings will have to be.

(6) So that two or more current drivers may operate the same core line at different times, the drivers should be open circuits when they are not being operated.

(7) The back voltage that will be developed across the load through which the current must be passed will oppose the current; and therefore, the load is one of the most important considerations. The back voltage which results from driving a line of cores may be considered to consist of four components[1, 2]:

(a) A voltage proportional to the current due to the resistance of the drive wire.

(b) A voltage proportional to the rate of change of the current due to the inductance of the drive wire.

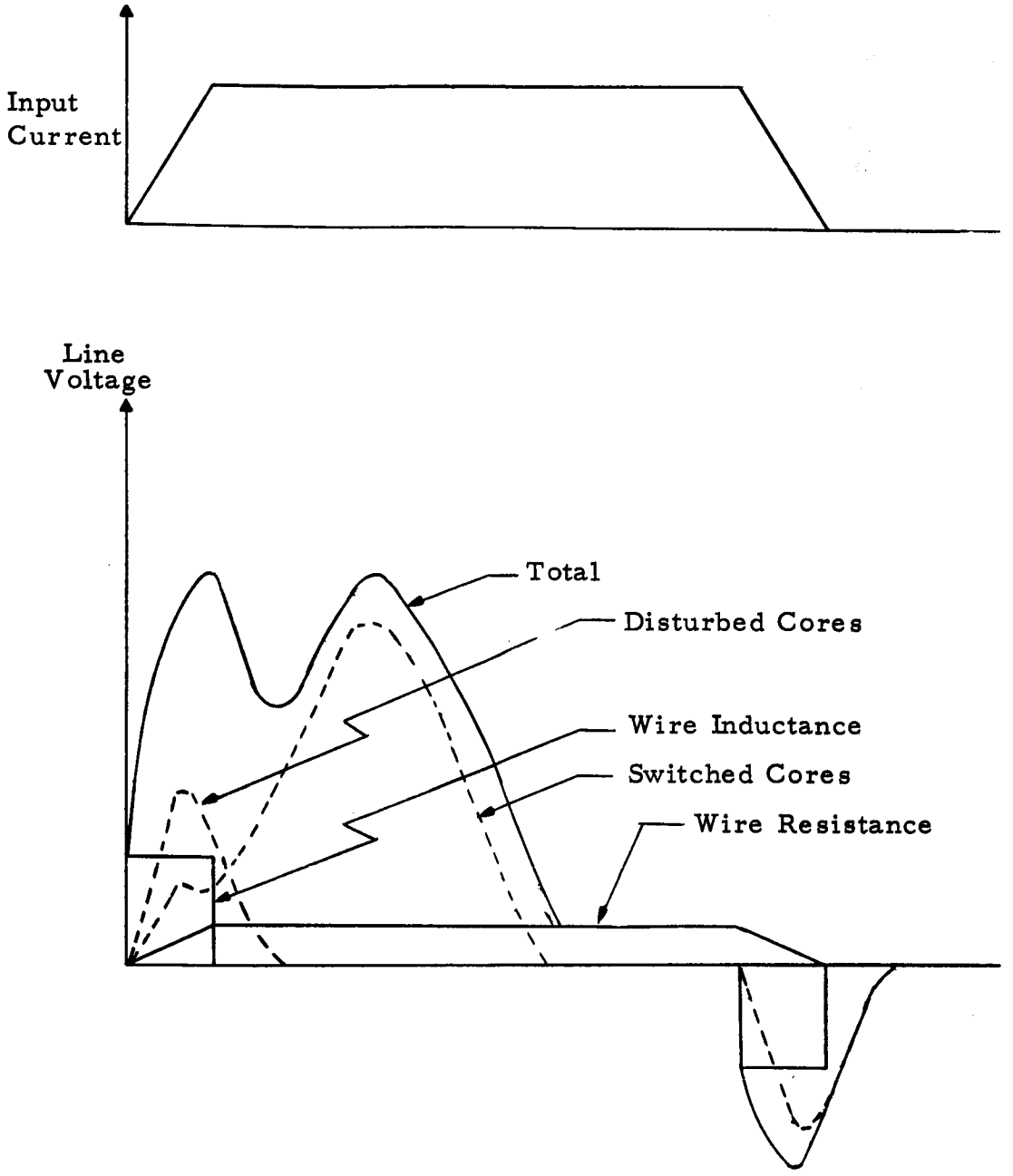


Fig. 6-1 Example of Back Voltage on a Core Line

6.2 Design Philosophy for Current Drivers

The discussion in this and the following section will be directed towards using transistors in current drivers, since these devices have been used extensively in the past for this purpose[3] and they are readily coupled to the usual forms of transistor and integrated logic circuitry. It is assumed that the reader has some knowledge of transistors, and there are many good references on the subject including References 4, 5, 6, and 13.

The current driver is a current source which may be switched on and off, and the current is derived from a power supply which may be represented as a voltage source, E, in series with a small source resistance R_s.

Fig. 6-2 is the general form of a current driver which may be used in certain instances. Connected across the power supply terminals is a current limiting resistor, R, in series with a switch S and a line of cores. The current, i, is zero when S is open, and when S is closed

$$i = \frac{E - v_c}{R_s + R} \qquad (6.2.1)$$

where v_c is the voltage across the core line and consists of the

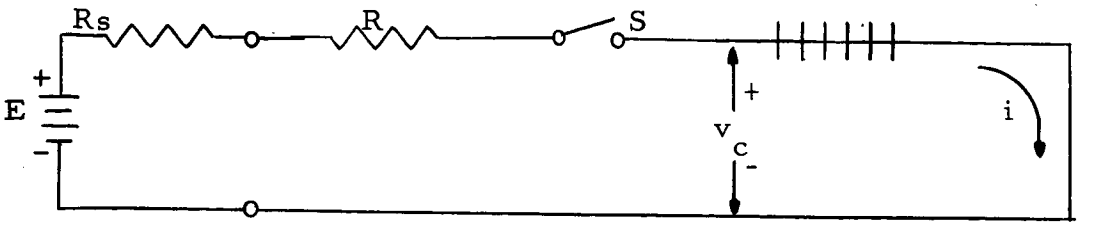
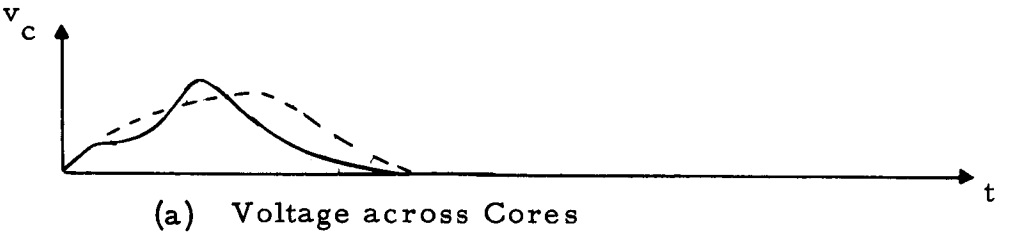
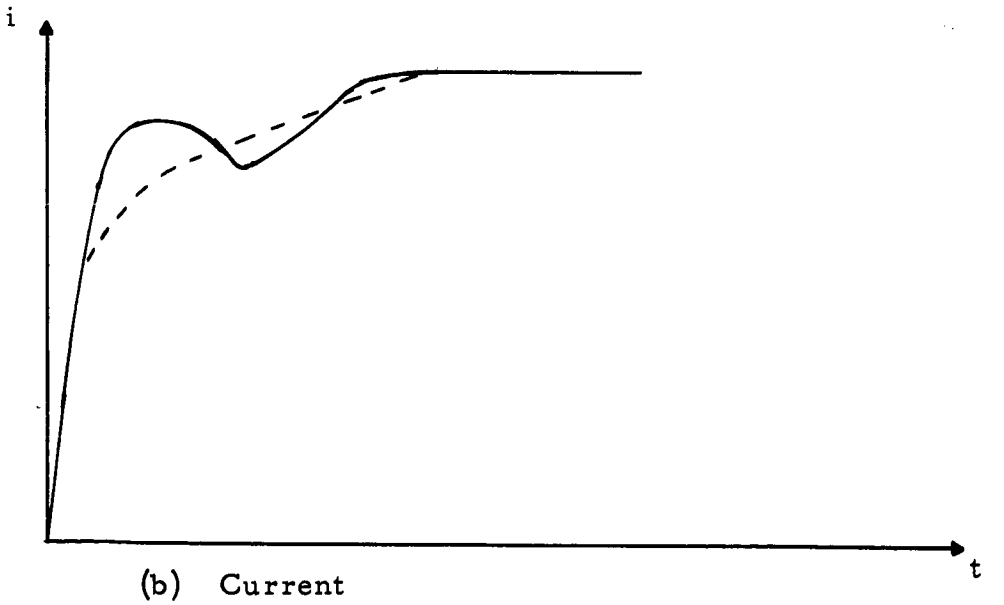


Fig. 6-2 Form of a Simple Current Driver



(a) Voltage across Cores



(b) Current

Fig. 6-3 Switching Transients in Circuit of Fig. 6-2

components listed previously. Thus, the current waveform is dependent upon v_c, but after all flux changes in the cores have occurred, v_c will be zero (if the line resistance is neglected) and the current will be

$$i = \frac{E}{R_s + R} \qquad (6.2.2)$$

which determines the final state to which the cores are driven.

Typical waveshapes that result from a driver of this type are illustrated in Fig. 6-3. Fig. 6-3a is the back voltage v_c, and Fig. 6-3b is the current. The initial rise of the current is due to the wire inductance, the initial voltage developed across the cores, the turn on time or rise time of the switch, and the inductance associated with R. The solid lines indicate the response when $E/(R+ R_s)$ is more than sufficient to switch the cores, and as a result a dip occurs in the current as the cores reach their maximum rate of flux change and v_c is at a maximum. The dotted lines indicate the case where the final value of current is just sufficient to cause switching; the dip vanishes, the rise time becomes longer, and the cores switch at a slower rate.

For a given drive current value, the degree to which the current is dependent upon v_c varies with the supply voltage

available. If E is much greater than the maximum peak value of v_c, then the effect of v_c will be minimal, and the behavior of a constant current generator will be approached. However, this will probably not be the case with transistor circuitry where power supply voltages are on the order of 10 or 20 volts. For example, if E is 10 volts, and there are 10 cores to be switched with each core producing a peak voltage of 0.10 volts, then the maximum v_c would be 10 per cent of E, and the current would vary 10 per cent as the cores switched.

The circuit, which can be readily built using a transistor as a switch, could be used for the following applications:

(1) as an inhibit or information current driver where speed is not too critical. In this application the back voltage will be small since at most one core on the line will switch. However, the rise time will probably be poor as there will be many disturbed cores on the line.

(2) as an addressing current driver in a low speed memories. There will be many switched cores on the line, the back voltage will be large, and the switching slow.

(3) as a read current source in a small LSM is possible, but the results will probably not be very good. The rise time will be rather poor, but it may be adequate for cores with long switching times. The final value of current, $E/(R_s + R)$, should be made much greater than that necessary to switch the cores so that the current during the period while the cores do switch will be great enough to give good output voltages.

Fig. 6-4 shows a typical transistor implementation of the circuit of Fig. 6-2. The input voltage, V_{in}, is normally held at ground, and the transistor is cut off by the voltage divider network, R_1 and R_2 which reverse biases the base-emitter junction. R_1 is chosen so that when V_{in} is switched to +V sufficient current flows through it to saturate the transistor as well as maintain the voltage drop of approximately E' volts across R_2. The current which then flows through the cores is the emitter current, I_E, the sum of the collector current and the base current.

$$I_E = I_C + I_B$$

or

$$I_E = \frac{E - [\, v_c + V_{EC}\,(sat)\,]}{R_s + R} + \frac{V - [v_c + V_{EB}(sat)\,]}{R_1} - \frac{[\, v_c + V_{EB}\,(sat)\,] + E'}{R_2} \qquad (6.2.3)$$

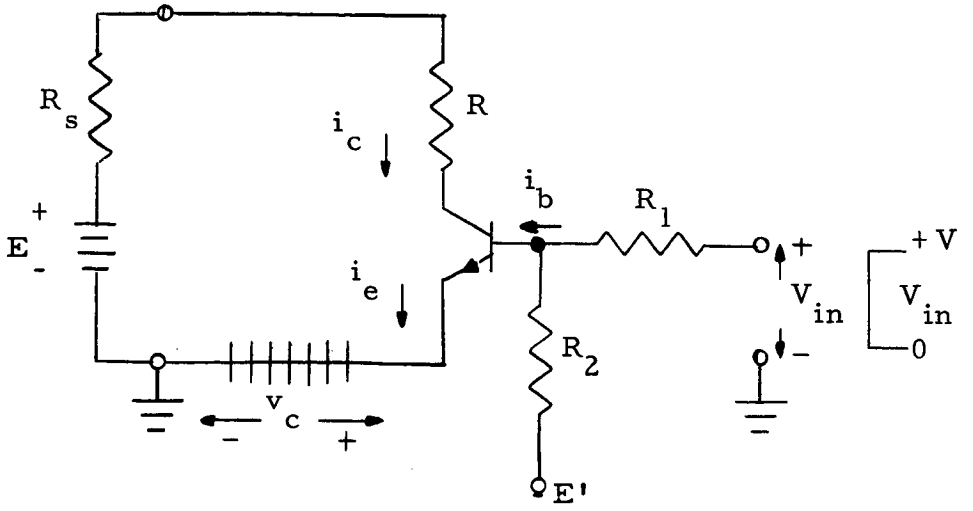


Fig. 6-4 Transistor Implementation of Fig. 6-2

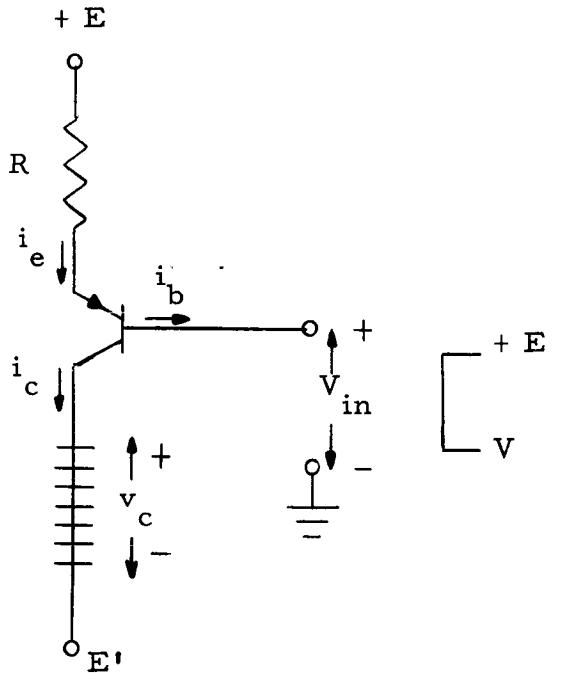


Fig. 6-5 Using a Transistor as a Switched Constant Current Source

where $V_{EB}(sat)$ is the emitter to base voltage at saturation, and $V_{EC}(sat)$ is the emitter to collector voltage also at saturation. Usually I_B will be small in comparison to I_C, R large compared to R_s, and $v_c + V_{EC}(sat)$ small (at least after the cores have switched) in comparison to E. Thus, for a first approximation

$$I_E \approx E/R \qquad (6.2.4)$$

From which it is clear that the tolerance of the final value of I_E is largely determined by the tolerance associated with R.

When the transistor is turned off by returning V_{in} to ground, the flyback voltage will cause v_c to go slightly negative. Also other currents in the memory threading some of the same cores or currents in lines having a common connection with the emitter of the transistor in question will also effectively cause v_c to vary. As a consequence, E', R_1, and R_2 must be chosen so that the base is held at a negative potential greater than any possible negative excursion of v_c; otherwise the transistor may become momentarily turned on. Also any positive excursion of v_c must be such that the emitter base breakdown potential rating is not exceeded.

By operating a transistor in the active region as a constant-current source, with the cores in the collector circuit and a current limiting resistor in the emitter circuit, a current driver whose output is essentially independent of the back voltage over a range may be built. The basic circuit configuration is shown in Fig. 6-5, and it is pointed out that other active devices such as a pentode vacuum tube may be used in place of the transistor.

In Fig. 6-5 the source resistance has been omitted, and for generality the core line has been returned to a supply voltage of E'. The circuit is controlled by V_{in} which is normally greater than or equal to $+E_C$ so that the transistor is held off. When V_{in} is switched to V with the constraint:

$$E > V > E' + v_c \qquad (6.2.5)$$

The transistor is biased in the active region. The emitter current is determined by V and R:

$$I_e = \frac{E - V_{in} - V_{BE}}{R} \qquad (6.2.6)$$

and the collector current through the cores is, neglecting the output admittance h_{oe} of the transistor

$$I_C = \frac{h_{FE}}{h_{FE} + 1} I_E \approx I_E \qquad (6.2.7)$$

where h_{FE} is the current gain (collector current/ base current) of the transistor. If β is much greater than one (and it usually is), then the emitter current is essentially equal to the collector current. Thus, the output current is constant as long as the transistor does not become saturated. Recall that saturation will occur when $V_{in} \leq E' + v_c$, and this fact is used in determining the proper V_{in}.

The current rise time will be determined by the frequency characteristics of the transistor (it was found experimentally that a transistor with gain-bandwidth products of 100 to 300 Mc or more will provide rise times of 0.20 μ sec or less) as well as the switching time of V_{in}. The circuit does not give any improvement in the rise and fall times of the control voltage, so it is necessary to have V_1 switch in at least the same time as the desired rise time. Also effecting the rise time is any inductance associated with R; using a carbon resistor is a low cost solution with minimum inductance.

From equations (6.2.6) and (6.2.7) it is seen that if the voltage supply is well regulated and the base-emitter characteristics

of the transistor are well known, the tolerance of the output current is primarily dependent upon the tolerance of R and the tolerance to which V_{in} may be generated. The transistor and supply voltages must be selected so that voltage changes at the collector due to flyback and other effects previously mentioned do not exceed the collector to base breakdown voltage or cause the collector-base junction to become forward biased when the transistor is being held off.

The two circuit configurations are now compared. The current waveform produced by the first circuit is highly dependent on the load which limits its use to low speed operations and where the voltage response of the core is not critical. The output of the switched constant current generator is close to the trapazoidal wave shape required for most read operations and all high speed operations. The advantage of saturating the transistor rather than operating it in the active region is in the power ratings required. For a pulse of given amplitude and duration, the saturated transistor will be required to dissipate less power than the nonsaturated one since the collector emitter voltage is much smaller. Hence, the nonsaturated transistor will require a higher power rating.

In both cores, the transistor that switches the current will probably have to be controlled by at least one more transistor before coupling to the output of a standard logic element to give current gain and/or rise time improvement.

As a final point, the currents that are dealt with in current drivers are on the order of a few hundred milliamperes which is several orders of magnitude greater than typical transistor leakage currents; and therefore, leakage currents may normally be ignored in the design and analysis of current drivers.

6.3 Examples of Current Drivers

6.3.1 Introductory Comments

The first step in the design of a current driver is to find a workable circuit configuration. Once this has been done, the selection of components to give the desired output is a fairly simple task involving the application of Ohm's law to worst case situations to find the allowable extremes in component values. This procedure is illustrated in the first design example; further examples of worst case designs of digital circuits are to be found in Reference 12 (Particularly in Part 4).

It is pointed out, however, that the selection of a particular circuit configuration may lead to impossible or undesirable component values for a particular output current. In such an event one has the choice of finding a new circuit configuration or of redefining the problem in such a manner as to allow new output requirements which are more readily achieved.

The third article of this Section reviews the design of the current drivers used to generate the oscillograms in Chapter 4, and the final article presents additional current driver circuit configurations.

Once the circuit has been designed on paper, it is advisable to build and test a bread board version of the circuit; and if necessary, improvements or modifications in the design can be made at this point. Oftentimes the selection of such components as speedup capacitors, timing capacitors and resistors and the like can be best made experimentally at this point (although the sophisticated circuit designer may prefer to calculate these values beforehand).

A point to bear in mind in the construction and testing of a current driver system is that a current driver will cause

large and abrupt changes in the output current of the system power supplies. Although the power supplies will undoubtedly be well regulated for slowly changing loads, it is to be expected that transient voltages will appear on the power supply bus lines when a current driver is switched on and off. These transients are disadvantages in that not only will they effect the shape of the output current but they may cause other circuits in the system (such as flip-flops and one shots) to give false outputs. The transients, however, can be minimized by placing bypass capacitors across the bus lines physically close to the current driver. Since the transients tend to be short in duration, the bypass capacitors should have a very low inductance associated with them so that they will readily pass high frequencies. It was determined that electrolytics are not very good in this regard, but tantulum and paper capacitors (on the order of several microfarads) are satisfactory with the tantalum capacitors being superior to the paper ones but more costly. Furthermore, small mica or ceramic capacitors can be used in parallel with larger capacitors to improve the high frequency filtering.

6.3.2 An Information Driver Using a Saturated Transistor Switch

The circuit of Fig. 6-6 was designed for use as an

information driver for a hypothetical small (about 50 words), relatively low speed memory. The design constraints were:

(a) output current: in the range of - 320 ma ± 10%

(b) maximum memory speed: one read/write cycle per 200 μ secs.

(c) maximum time alotted for writing: 20 μ sec

(d) switching speed of core: less than 3 μ sec with long rise times

(e) the input signal will come from a gated pulse generator[7] (shown in Fig. 6-7) which ANDs a level representing the information to be written and a pulse which is the write command.

(f) available power supplies are -12 volts and +6 volts

The first four constraints suggest that a saturated transistor switch operating between the -12 volt supply and ground will provide a workable solution. A silicon, PNP, 2N3638 transistor was selected for the switch because of its low cost (31 cents), collector current rating (500 ma), power rating (500 mw), and high gain-bandwidth product (over 100 mc) at high currents which implies a fast turn on time. The minimum β at a collector current of 300 ma is 20, and the emitter to base breakdown voltage

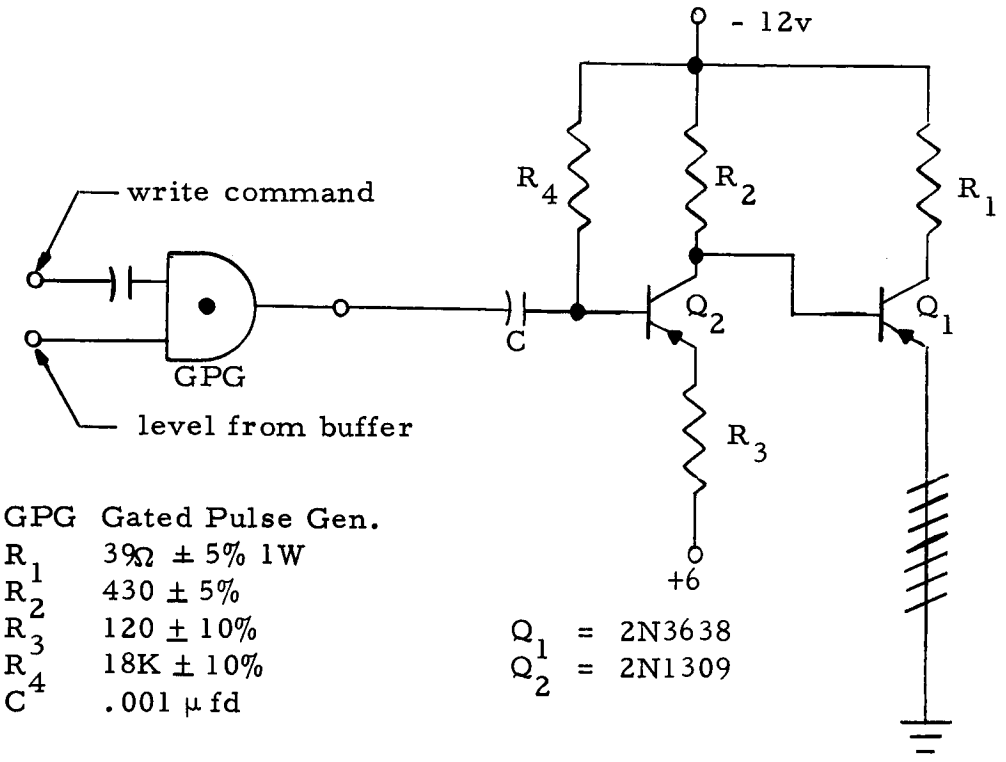


Fig. 6-6 Information Current Driver with Output of 320 ma ± 10%.

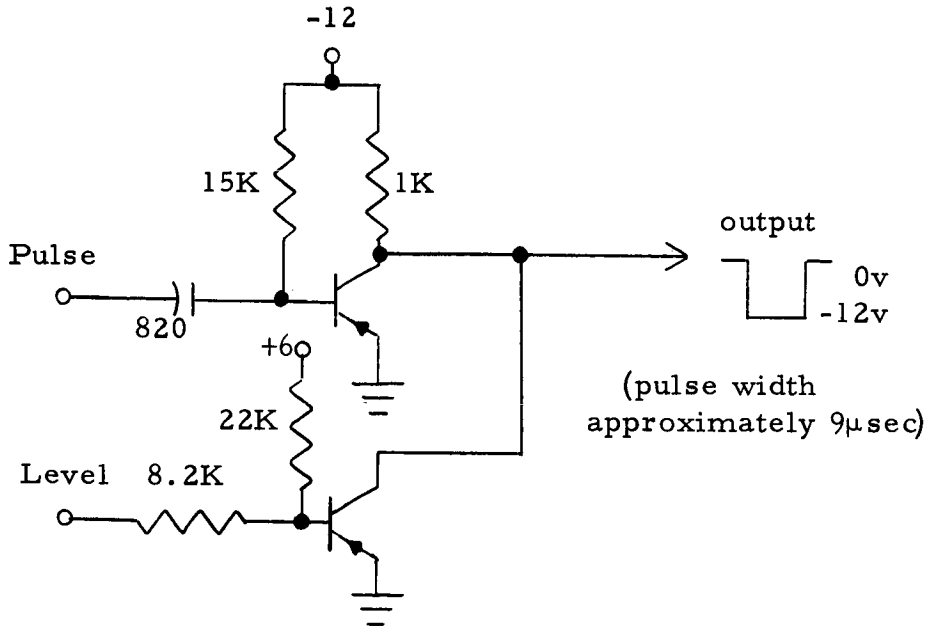


Fig. 6-7 Gated Pulse Generator[7]

(BV_{EB0}) is -4v.

The low current gain and BV_{EB0} suggested that the control circuit configuration shown would be more desirable than that indicated by Fig. 6-4. (In Fig. 6-4, R_1 would have to be small, about 500 ohms, in order to saturate the transistor. R_2 would have to be returned to +6v and be of the same order of magnitude as R_1 to sufficiently reverse bias the base-emitter junction. Considerable current would therefore have to be supplied to R_2 to maintain the 6v drop across it when the transistor is turned on.)

The circuit works in the following manner: Q_2 is normally saturated by the current in R_4. R_2 and R_3 are selected so that the collector of Q_2 is normally at a voltage of approximately + 2.5v; thus, cutting off Q_1. When the output current is to be produced, the gated-pulse generator produces a negative going pulse (from ground to -12v) that is 5 to 10 μsec long. The leading edge of the signal sees a low impedance path through the base of Q_2 to ground, but the positive-going, trailing edge of the signal drives the base of Q_2 positive cutting the transistor off. Base current is then applied to Q_1 through R_2 turning it on. The base voltage of Q_2 decays exponentially with a time constant of R_4C; when it decays below +6v, Q_2 turns on again and Q_1 turns off.

The component values are now determined step-by-step, and while the output is designed to be in the range of 320 ma ± 10%, the procedure followed is general enough to allow one to design for another value of output current. RETMA standard values will be used wherever possible. Since the memory is small, the impedance of the drive wire will be neglected.

(1) Determine R_1: Most but not all of the output current, I, will flow through R_1. Hence

$$R_1 > \frac{V_{cc} - V_{CE}(sat)}{I} \approx \frac{12 \text{ volts}}{320 \text{ ma}} = 37.5 \text{ ohms}$$

R_1 is tentatively chosen as 39 ohms ± 5%. The 5% tolerance is necessary since the output will not be centered at 320 ma.

(2) The worst case collector currents, I_C, are now calculated from

$$I_{C_{min}} = \frac{V_{cc} - V_{CE}(sat)_{max}}{R_{1_{max}}} = \frac{12 - V_{CE}(sat)_{max}}{41}$$

$$I_{C_{max}} = \frac{V_{cc} - V_{CE}(sat)_{min}}{R_{1_{min}}} = \frac{12 - V_{CE}(sat)_{min}}{37}$$

From the specification sheet for the 2N3638 transistor it is seen that $V_{CE}(sat)_{max} = -1v$, and $V_{CE}(sat)_{min}$ may be taken as zero. So $I_{C_{min}} = 268$ ma, and $I_{C_{max}} = 324$ ma

(3) The worst cases for the base current I_B are now determined.

First of all the sum of I_B and I_C must be within 320 ma ± 10%; or

$$|I_{C_{min}}| + |I_{B_{min}}| > 320 \text{ ma} - 10\% = 288 \text{ ma}$$

and $$|I_{C_{max}}| + |I_{B_{max}}| < 320 \text{ ma} + 10\% = 352 \text{ ma}$$

Using the results of (2) we have:

$$|I_{B_{min}}| > 20 \text{ ma and } |I_{B_{max}}| < 28 \text{ ma}$$

Furthermore, the minimum I_B must be sufficient to saturate the transistor when I_C is a maximum. Since the minimum β is 20,

$$|I_{B_{min}}| \geq \frac{|I_{C_{max}}|}{\beta_{min}} = \frac{324}{20} = 16.2 \text{ ma}$$

which is less than the value previously determined. Thus, the limits on I_B are $20 < I_B < 28$ ma.

(4) Determine R_2: The base current flows entirely through R_2, and the potential across R_2 is $V_{CC} - V_{EB}(sat)$. The worst cases for I_B are found as

$$I_{B_{min}} = \frac{V_{CC} - V_{EB}(sat)_{max}}{R_{2_{max}}}$$

$$I_{B_{max}} = \frac{V_{CC} - V_{EB}(sat)_{max}}{R_{2_{min}}}$$

Therefore

$$R_{2_{max}} \leq \frac{V_{CC} - V_{EB}(sat)_{max}}{I_{B_{min}}}$$

$$R_{1_{min}} \geq \frac{V_{CC} - V_{EB}(sat)_{min}}{I_{B_{max}}}$$

From the transistor specification sheet the limits on $V_{EB}(sat)$ are $0.8 \leq V_{EB}(sat) \leq 2.0$ volts, and the limits on R_2 become $400 < R_2 < 500$ ohms. Thus R_2 may be selected as 430 ohms $\pm$ 5%.

Note, that if the allowable spread in I_B at this stage

was not sufficient to allow a reasonable value for R_2 to be selected, it would be necessary to go back to the first step and pick another R_1.

(5) Determine R_3: When Q_2 is saturated its collector voltage is (neglecting the collector to emitter voltage and base current) approximately

$$V_{C2} \approx 6 - \frac{18\, R_3}{R_2 + R_3}$$

R_3 must be chosen so that V_{C2} is sufficiently positive to hold Q_1 off without exceeding the emitter-base breakdown voltage of BV_{EB0} = 4 volts for Q_1. The limits $+1 < V_{C2} < +3$ volts are imposed to fulfill these conditions. Since

$$V_{C2_{max}} = 6 - \frac{18\, R_{3_{min}}}{R_{2_{max}} + R_{3_{min}}}$$

and

$$V_{C2_{min}} = 6 - \frac{18\, R_{3_{max}}}{R_{2_{min}} + R_{3_{max}}}$$

Using the value of R_2 previously decided upon, the limits on R_3 are found as

$$R_{3_{max}} = \frac{(6 - V_{C2_{min}}) R_{2_{min}}}{(12 + V_{C2_{min}})} = 157 \text{ ohms}$$

$$R_{3_{min}} = \frac{(6 - V_{C2_{max}}) R_{2_{max}}}{(12 + V_{C2_{max}})} = 90.4 \text{ ohms}$$

R_3 is therefore selected as 120 ohms ± 10%. It will be necessary to check this value after Q_2 and R_9 have been determined, to ensure that the collector to emitter voltage and the base current do not adversely effect the selection.

(6) Select Q_2: When Q_2 is switched off by a 12 v, positive-going transition, the emitter to base voltage will be at most -22v. When it is on the collector current will be $18/(R_2 + R_3) \approx 25$ ma. And as stated previously, it is desirable that R_4 be large so that C may be small which implies that a reasonably high β is necessary. A Germanium PNP, 2N1309 fills all of the above requirements at a reasonable price.

(7) Determine R_4: When Q_2 is saturated the voltage drop across R_2 will be approximately the same as the voltage drop across R_4, and the current in R_4 multiplied by the minimum β must exceed the current in R_2. Thus, the requirement

$$R_{4_{max}} < R_{2_{min}} \beta_{min} = 408\, \beta_{min}$$

must be satisfied to ensure saturation. The specifications for the 2N1309 show a minimum β of 80 at a collector current of 10 ma, and a minimum β of 20 at 200 ma. A safe assumption for the minimum β at the collector current being used is 55, and the constraint on R_4 becomes $- R_{4_{max}} < 22.4K$. Thus, R_9 is selected as $18K \pm 10\%$.

Now the current drawn by R_4 is less than 1 ma, and the collector-emitter voltage for the saturated 2N1309 is, from the specifications, less than 0.2 v. The assumptions made in step 5 are therefore valid, and it is not necessary to adjust the value of R_3.

(8) Determine C: The base of Q_2 is normally at about 2.5 v. The positive going input transition causes the base to go positive to + 14.5 v; the voltage then decays exponentially with a time constant of R_4C towards -12v. Thus, the voltage $v_B(t)$ can be written as a function of time after the positive going input has been applied.

$$v_b(t) = 26.5\, e^{-t/R_4C} - 12$$

when the input has decayed to +6 v, the transistor starts to turn on again. To allow for the output current rise time and for the one core on the line to switch, a minimum pulse width of 5 μ sec may be decided upon. So at t = 5 μ sec, v_b should be a minimum of 6 volts. These values are substituted into the equation for v_b to find the minimum time constant:

$$R_{4_{min}} C_{min} = \frac{t}{v_B + 12 - n\left(\frac{}{26.5}\right)} = \frac{5 \times 10^{-6}}{-\ell n\,(0.68)} \approx 13\,\mu\text{ sec}$$

or

$$C_{min} > \frac{13 \times 10^{-6}}{16.2 \times 10^{3}} = 805 \text{ pf}$$

The final selection for C is 0.001 μf ± 10%.

(9) Determine Resistor Power Ratings: Calculating the power dissipated in R_2, R_3, and R_4 when the circuit is in its normal state (Q_2 on) shows that the ratings for these resistors must be at least 1, 1/2, and 1/4 Watts respectively. The average power dissipated by R_1 assuming Q_1 will be turned on for 10 μ sec, once every 200 μ sec, is about 0.2 Watts. There is, however, no guarantee that a resistor of the same rating will survive under

these operating conditions[8], so a 1 Watt resistor is selected.

6.3.3 Current Pulse Generators for a Memory Core Tester.

The circuitry described here was used to generate the current pulse trains described in Chapter 4, and the actual outputs are those shown in the oscillograms of Figs. 4-6 through 4-8. Four current pulse generators are required (one for full read currents, one for half read, one for full write, and one for half write), and their outputs are connected together as shown in the block diagram, Fig. 6-8. The common output is passed through the core under test and thence a small, non inductive, current sensing resistor to ground. The current drivers are designed to respond to signals from the Digital Systems Synthesizer described by P.M. Vargo[9] or from the outputs of the Wang Laboratories, Inc., Programmed Pulse Generator, Model 612AT. In either case these are the signals previously described. A logic circuit may be built using the Digital Systems Synthesizer to select one of the current generators at a time and thus form a train of pulses. However, using the Digital Word Generator - which has two independent, recycling, programmable, serial outputs as well as outputs that occur for a particular clock time of the output cycle- is more convenient to use and was used in the generation of the

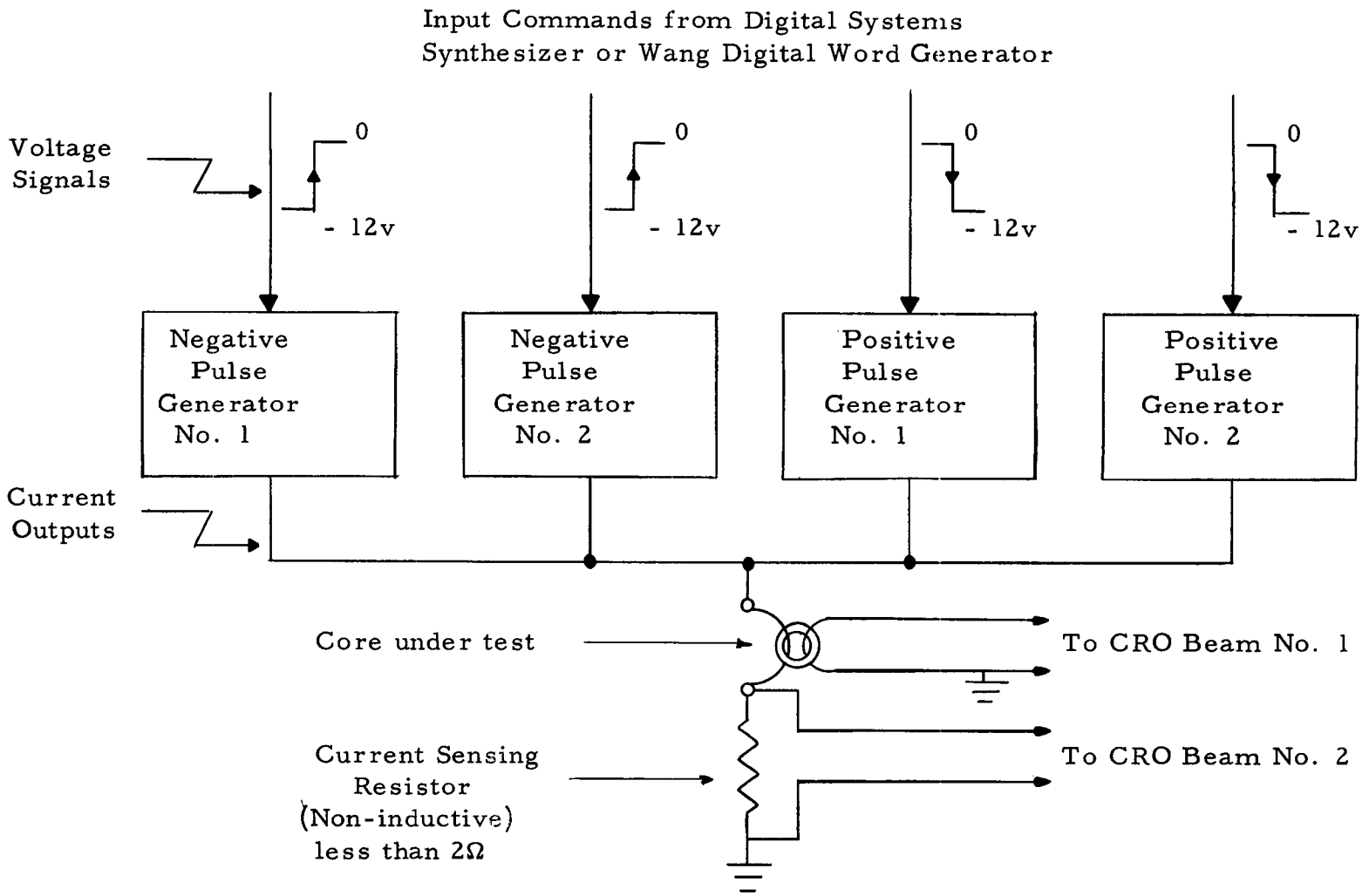


Fig. 6-8 Block Diagram of Memory Core Tester

oscillograms in Chapter 4.

The design considerations are:

(1) independent control of the rise time, duration, and amplitude of the output of each generator, and these quantities are to be in the range generally used with memory cores.

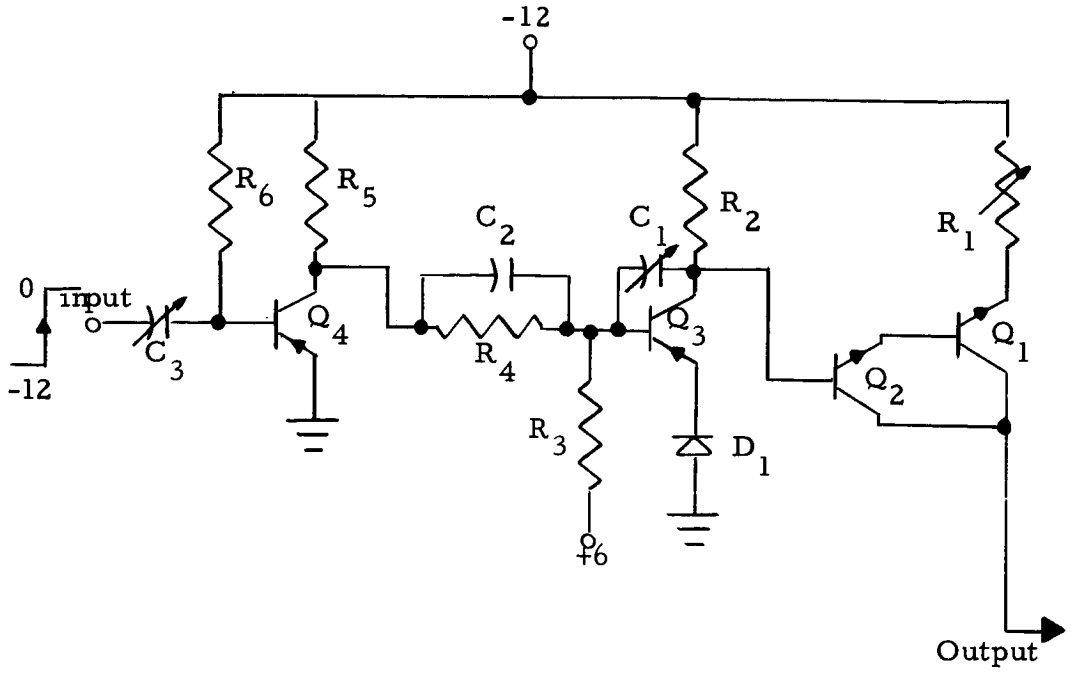
(2) The output should be independent of the back voltage produced by the one core under test and the current sensing resistor.

(3) The supply voltages available are -12v and +6v.

(4) The current rise should be nearly linear.

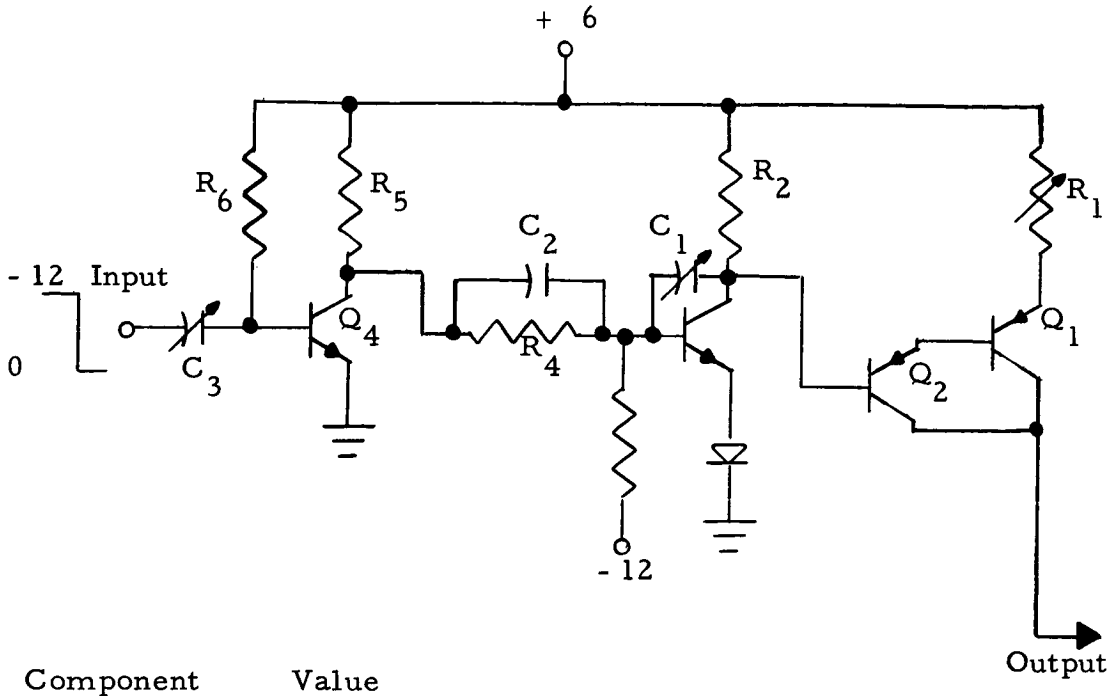
The negative and positive pulse generators are shown in Figs. 6-9 and 6-10. Both circuits are functionally the same; and hence, only the negative pulse generator will be described.

Transistors Q_1 and Q_2 are connected in a Darlington configuration and act as a single transistor with a β of approximately the product of the β's of the two individual transistors, $\beta_1 \beta_2$[10]. The output is taken from the collector to fulfill consideration 2; and its amplitude is controlled by the variable resistance R_1. 2N3704 transistors were chosen for use because of their high



Component	Value
R_6	27K, 10%
R_5	1K, 10%
R_4	8.2K, 10%
R_3	28K, 10%
R_2	2.2K, 10%
R_1	See Fig. (6-11)
C_3	approx. 300 pf
C_2	82 pf
C_1	20 ~100 pf
Q_4	2N1309
Q_3	2N3638
D_1	1N456
Q_1, Q_2	2N3704

Fig. 6-9 Negative Pulse Generator for Core Tester



Component	Value
R_1	
R_2	2.2K, 10 %, 1/4W
R_3	56K, 10 %, 1/4W
R_4	8.2K, 10 %, 1/2W
R_5	1K, 10 %, 1/2W
R_6	27K, 10 %, 1/2W
C_1	20 to 100 pf
C_2	82 pf
C_3	approx. 300 pf
D_1	IN456
Q_1, Q_2	2N3638
Q_3	2N3704
Q_4	2N1304

Fig. 6-10 Positive Pulse Generator for Core Tester

gain bandwidth product (over 100 mc) and their high current carrying capabilities (800 ma, 400 mw); also they are silicon transistors so that the leakage currents will be very small. The Darlington configuration was chosen for use primarily because the input impedence to the base of Q_2 will be approximately $\beta_1 \beta_2 R_1 > 400 R_1$, if the minimum β is 20; and it will not seriously load the collector voltage of Q_3 which controls the pair.

Transistor Q_3 together with the feedback capacitor C_1 is a Miller integrator[11]. It is normally cut off holding the Darlington pair off; the only output current will then be small leakage currents on the order of a few micro amperes or less. When Q_3 is fully on, the collector voltage is approximately at -1v (due to the 0.7 v drop across the silicon diode D1 and a drop of approximately 0.3v across the saturated transistor); this allows the collectors of Q_1 and Q_2 to go to a negative potential of 1 v before saturation. When Q_3 is turned on or off, the voltage across R_1 will follow the collector voltage; and because of C_1 the collector voltage change will be nearly linear with time. The output current will therefore rise and fall nearly linearly, and varying C_1 will vary the rise and fall times.

Q_4 is normally saturated by the current in R_6, and it holds Q_3 off. A positive going voltage transition at the input turns Q_4 off for a time determined by the time constant R_6C_3. When Q_4 is cut off, Q_3 is turned on; and varying C_3 will vary the duration of the output current. A 2N972 Germanium transistor was chosen for Q_3 because of its high frequency characteristics. The frequency characteristics of Q_4 are not as critical, and a 2N1309 was selected for use. R_2, R_4, R_5, and speed up capacitor C_2 were chosen (partially by experimentation) to give an output current rise time of less than 0.03 μsec with R_1 approximately 12 ohms (which gives an output current of approximately 750 ma considering at least a 0.7 v drop across the base-emitter junctions of both Q_1 and Q_2) and with C_1 removed. R_3 and R_6 are then readily determined to reverse bias Q_3 and to saturate Q_4 respectively. The final values are given in the Figure. With C_3 on the order of 300 pf gives output pulse durations on the order of 10 μsec.

The scheme of Fig. 6-11 was used to obtain a variable resistance for R_1 with minimum inductance. The 2P5T switch allows coarse adjustment from 3.9 to 61 ohms in five overlapping steps. The potentiometer allows fine adjustment within each step by shunting part of the fixed resistance. The fixed resistors

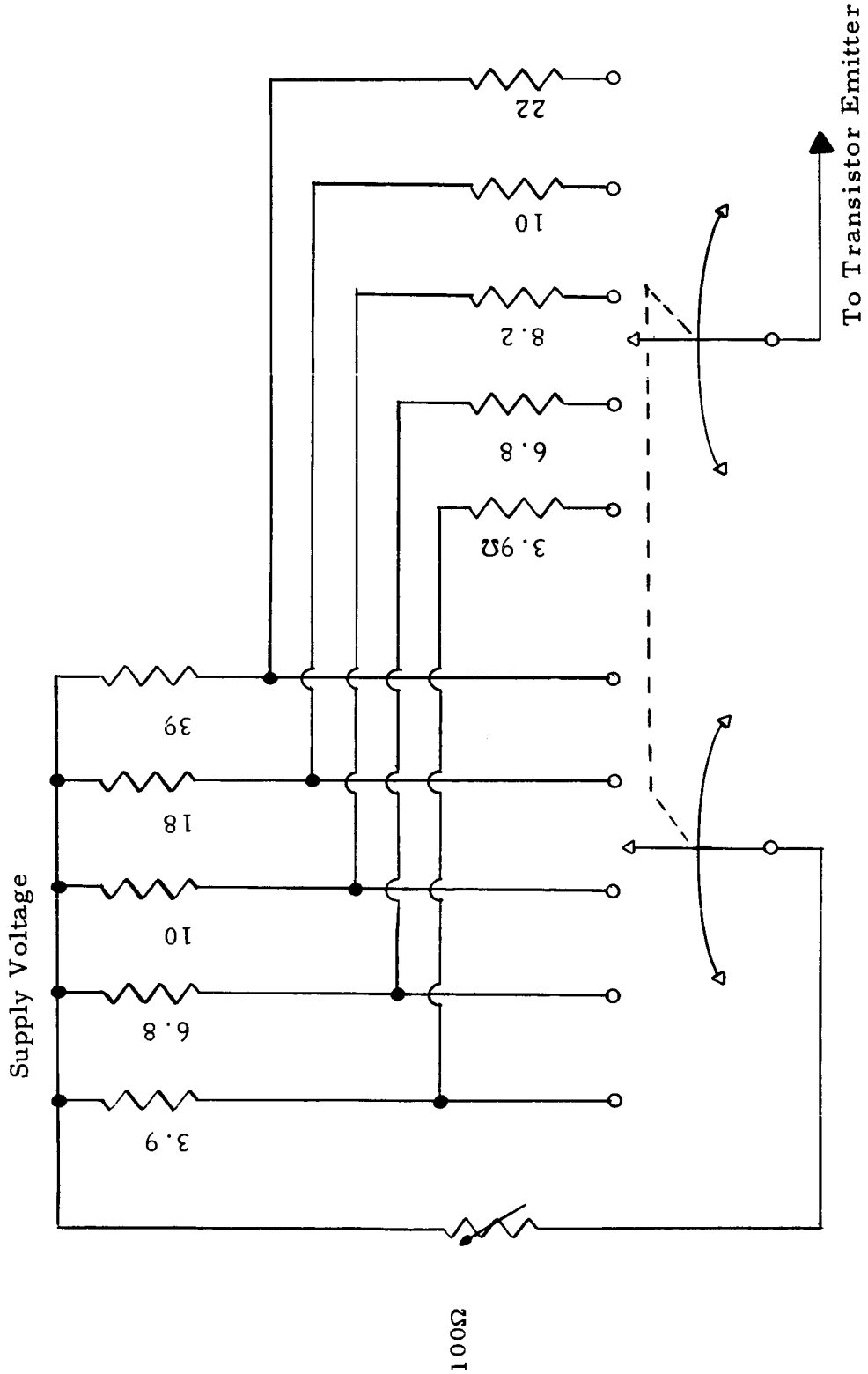


Fig. 6-11 Method of Achieving Variable Resistance

are carbon composition, and the potentiometer is wire wound. Potentiometers with a maximum resistance of from 100 ohms to 1K ohms are satisfactory. The chief reason for using this arrangement was that the equipment was readily available. Perhaps a more satisfactory solution would be the use of a non-inductively wound potentiometer.

6.3.4 Other Current Driver Circuit Configurations

(a) Use of a pulse transformer - Two problems that occur in using a saturated transistor as a switch - as in Section 6.3.2 - are that the base current is a significant part of the output current and that during turn-on and turn-off the potential of the emitter relative to ground may vary quite widely which adversely effects the control current through the base. If these features prove undesirable a pulse transformer may be used as shown in Fig. 6-12. The input signal is applied to the base circuit of Q_1, and it turns Q_1 on. The resultant variation in collector voltage is transformed to the base of Q_2 turning Q_2 on. All of the base current of Q_2 circulates through the transformer secondary, and no base current flows to the line of cores. Because the transformer also provides dc isolation, the base current of Q_2 will not vary with changes in the potential of Q_2's emitter. Thus it is

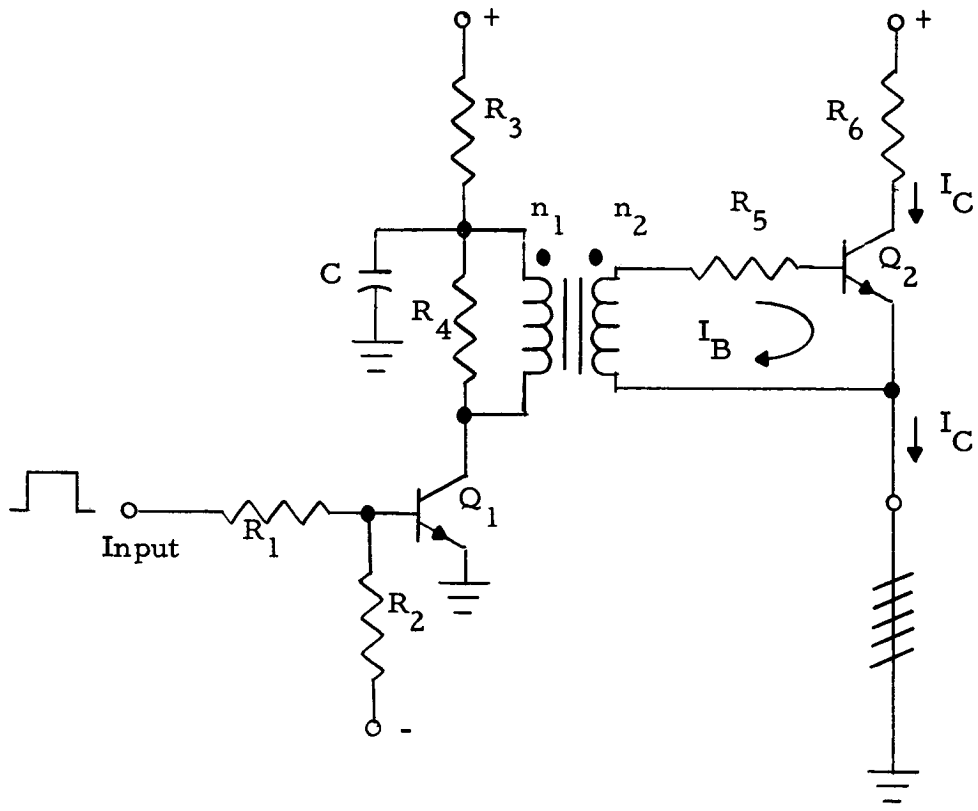
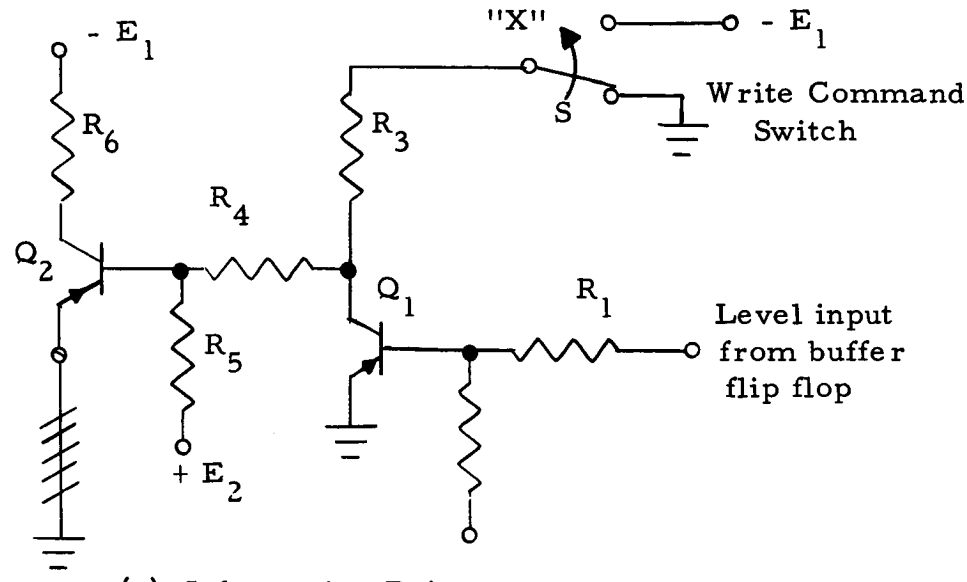


Fig. 6-12 Illustrating the Use of a Pulse Transformer to Control a Saturated Transistor Switch

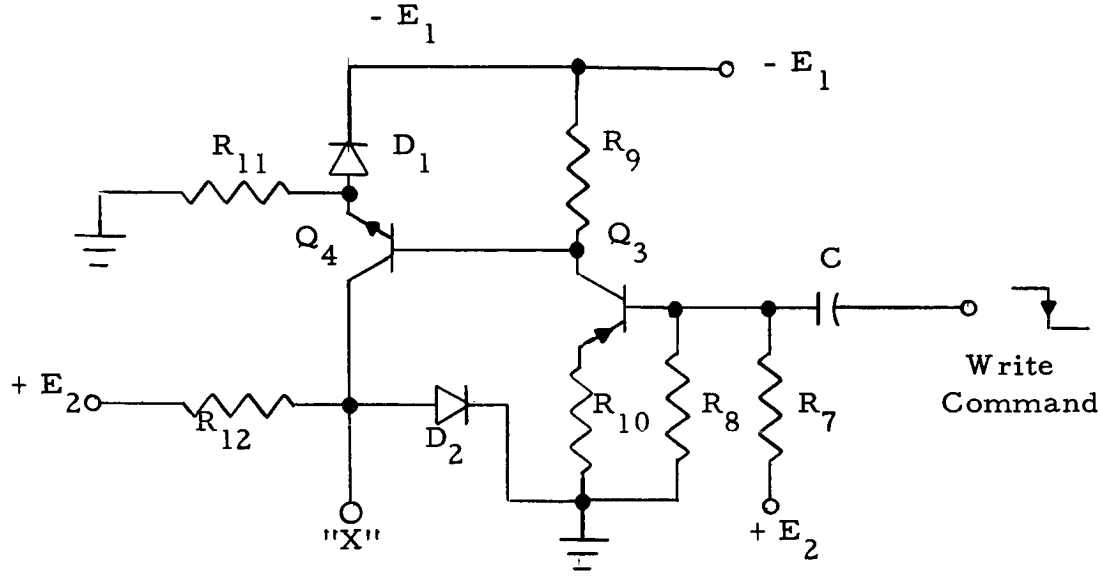
possible to deliver a large base current to Q_2 to ensure good saturation without worrying about its effect on the output current. In order to provide sufficient base current to Q_2 the turns ratio n_2/n_1 may be made less than unity; this is entirely possible since a relatively small base-emitter voltage is required to turn Q_2 on.

Since the d-c impedance of the pulse transformer is quite low, R_3 is used to limit the collector current of Q_1 after the transient effects, resulting from turning Q_1 on, have gone to zero. The capa citor, C, is charged to the positive supply voltage prior to turning Q_1 on, and C allows a voltage equal to the supply voltage to be developed across the transformer primary as Q_1 is turned on. R_4 is used for damping, and it may be chosen so that the RLC circuit will be critically damped. Thus R_4 is used to prevent ringing and to prevent a large (and possibly harmful) flyback voltage when Q_1 is turned off. R_5 is used to limit the base current of Q_2; and if the turns ratio is properly chosen, it may be possible to eliminate R_5.

(b) An Information driver scheme for a low speed LSM- Fig. 6-13(a) shows an information driver for a low speed LSM with writing by augmenting currents. The switch S acts as the

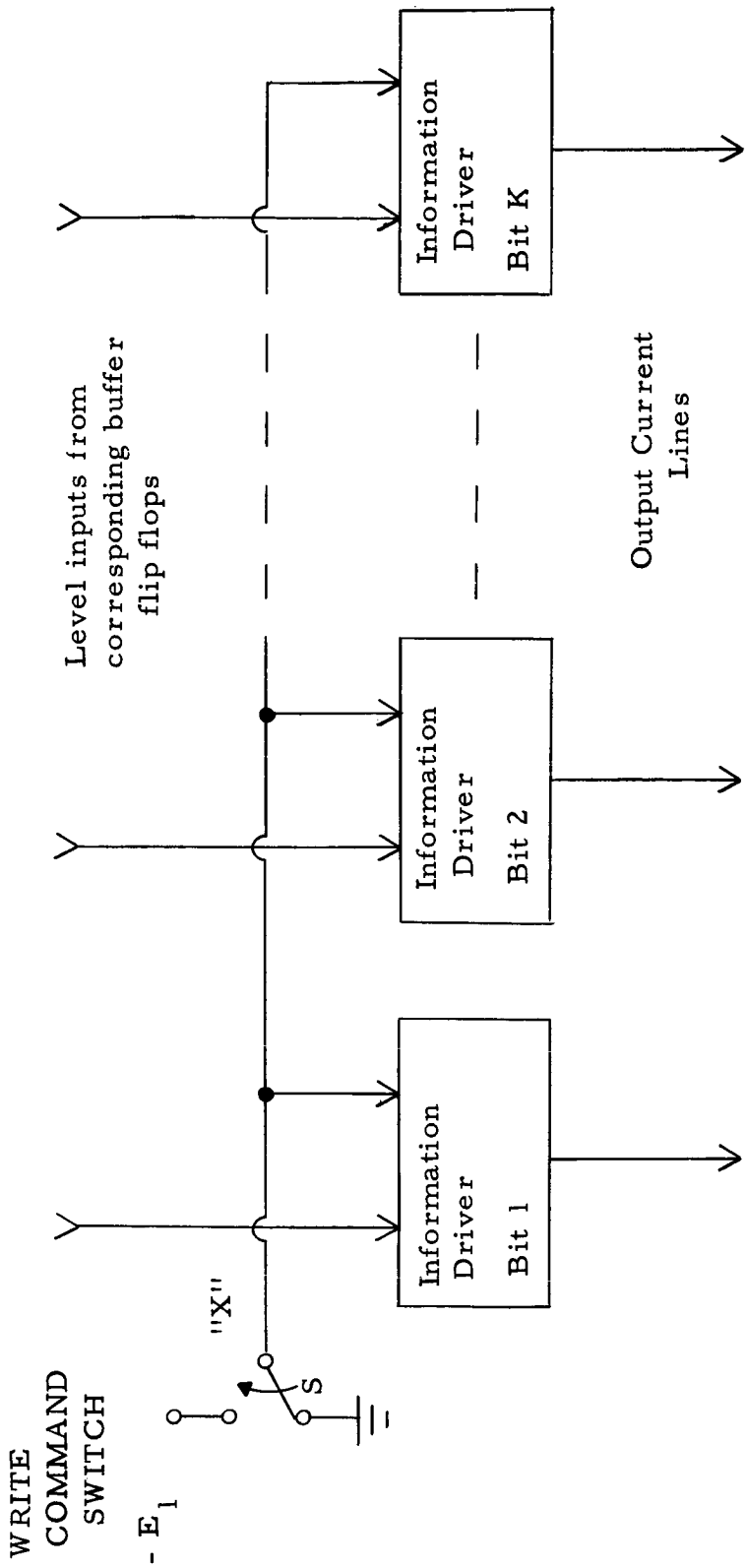


(a) Information Driver



(b) A Transistorized Implementation of the Switch in (a)

Fig. 6-13 An Information Driver Scheme for a Low Speed LSM



(c) Block Diagram Showing Connection of Several Drivers to a Single Write Command Switch

Fig. 6-13 (Cont.)

write command, and a suitable transistorized implementation of the required switch is given in Fig. 6-13b. S switches the point "X" from ground to $-E_1$, and it is common to all of the information drivers in the memory system as indicated by the block diagram in Fig. 6-13c.

The level input controls O_1; and as a result, it controls the information to be written. A negative input level saturates Q_1, but an input of zero volts causes Q_1 to be cut off. The switch is normally i the position that maintains point "X" at ground which holds Q_2 off. When a word is to be written, point "X" is switched to $-E_1$, and Q_2 will conduct if Q_1 is off. However, if Q_1 is saturated, Q_2 will be held off regardless of the position of S. Thus for writing by augmenting currents, an input level of zero volts will cause a one to be written, and a negative input level causes a zero to be written.

The operation of the switch circuit, Fig. 5-13b, is now described. Q_4, which is normally held off, replaces the actual switch contact; and Q_3 controls Q_4. R_{12} and D_2clamp the collector of Q_4, point "X", at approximately +0.7v (if a Silicon diode is used) when the transistor is off. D_1 and R_{11} maintain the emitter of Q_4 at $-E_1$ + 0.7v always. Q_3 is normally held off by a positive

voltage applied to its base through the voltage divider composed of R_7 and R_8; this fixes the base of Q_4 at $-E_1$ causing its base-emitter junction to be reverse biased. The write command, a negative going voltage transition, turns Q_3 on which turns Q_4 on. When Q_4 is saturated, its collector voltage will be approximately equal to its emitter voltage, and therefore point "X" will be at approximately $-E_1$ volts as desired. (D_2 will of course be reverse biased). The base current of Q_4 is limited by the emitter resistor, R_{10}, of Q_3. Q_3 and Q_4 will remain on until the timing capacitor, C, has charged to a point where insufficient base current flows to hold Q_3 on.

Table 6-1 lists component values for the circuits of Fig. 6-13 with the conditions stated.

(c) An emitter-coupled, regenerative current driver*

The circuit configuration in Fig. 6-14 has been successfully used as a read current generator in a small LSM. The common emitter connection to R_5 provides positive feedback (or regeneration) in the same manner as in a Schmitt Trigger circuit with the result

*

The initial development of this circuit is the work of D. Vlack of the Digital Systems Laboratories.

Table 6-1

Components used with circuits of Fig. 6-13 with the conditions:

(1) There will be 18 information drivers.

(2) The desired output current is -305 ma ± 80%.

(3) The time duration is to be 10 to 15 μ sec.

(4) Available Power Supplies are -12v and +6v.

(5) The logic levels are ground and -12v.

(6) The write command signal is a negative going 12v transition.

Component	Value	Comment
Q_1	2N1309	
Q_2	2N1998	
Q_3	TI411	
Q_4	2N1309	
D_1	1N4001	
D_2	1N456	
R_1	3.9 K	10%
R_2, R_{11}	8.2 K	10%
R_3, R_4	470 ohms	10%
R_5, R_{12}	6.8 K	10%
R_6	39 ohms	5% 1W
R_7	82 K	10%
R_8	22 K	10%
R_{10}	180 ohms	10%
C	470 pf	

that very short rise times can be obtained. The output is taken from the collector of Q_2, and the base of Q_2 may be damped to approximately $-E_3$ volts. Thus the circuit configuration can be readily adapted to such purposes as reading and writing in high speed memories including CCM's.

Q_1 is normally saturated by the current in R_2. Diodes D_2 and D_3 are then reverse biased, and the base of Q_2 is at approximately $-E_2$ volts by virtue of R_4 which is a sink for Q_2's leakage current. Since the emitter current of Q_1 flows through R_5, the emitter of Q_2 is slightly positive with respect to $-E_2$; and consequently, the base-emitter junction of Q_2 is reverse biased. A negative going input transition turns Q_1 off for a time determined by the timing circuit composed of R_1, R_2, and C_1. When Q_1 is off, the current through R_3 is diverted to the base of Q_2 which causes Q_2 to conduct. The components may be selected so that when Q_2 conducts, its base is clamped at $-E_3 + V_{D3}$, where V_{D3} is the forward voltage drop that occurs across D_3 when it conducts. This keeps Q_2 in the active region and allows for a back voltage of approximate magnitude $|E_4| + |E_3|$.

The pertinent relations - to which worst case conditions may be applied - are:

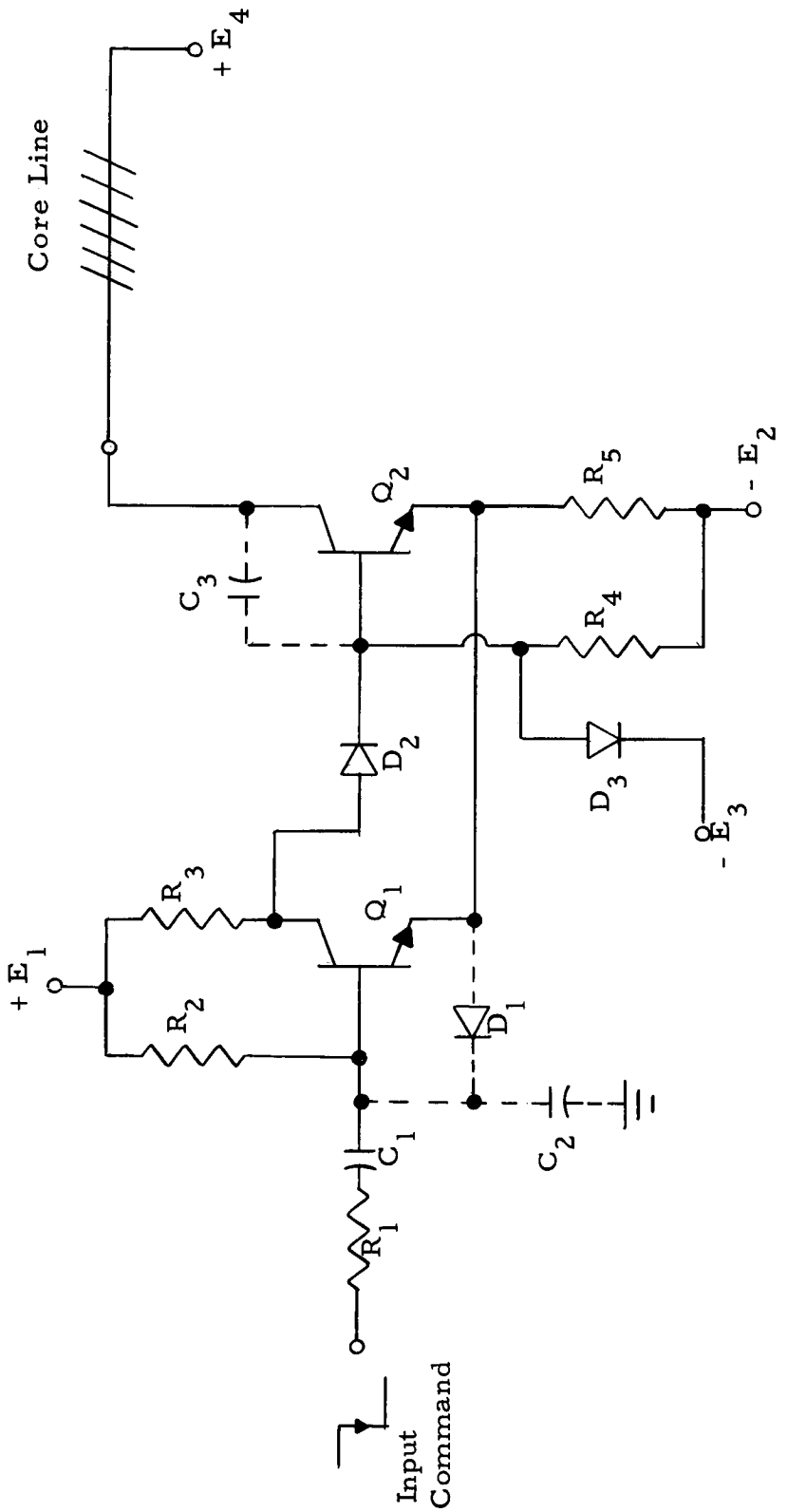


Fig. 6-14 Emitter-Coupled, Regenerative Current Driver

Note: $|E_2| > |E_3|$

1) to saturate Q_1

$$h_{FE1} R_3 > R_2$$

where h_{FE1} is the common-emitter current gain of Q_1.

2) to clamp the base of Q_2 at $-E_3 + V_{D3}$

$$\frac{E_1 - V_{D2} - V_{D3} - (-E_3)}{R_3} > \frac{(-E_3) + V_{D3} - (-E_2)}{R_4} + \frac{I_C}{h_{FE2}}$$

where I_C is the desired collector current and h_{FE2} is the current gain of Q_2.

3) and to produce the desired output current

$$\left(\frac{h_{FE2}}{h_{FE2}+1}\right)\left(\frac{V_{B2} - V_{BE2} - (-E_2)}{R_5}\right) = I_C$$

where V_{BE2} is the base-to-emitter voltage drop of Q_2 which occurs when Q_2 conducts and V_{B2} is the voltage applied to the base of Q_2 with respect to ground.

Shown in dotted lines are the optional components D_1, C_2, and C_3. D_1 is used to protect the base-emitter junction of Q_1 when Q_1 is turned off. C_2 acts as a speed up capacitor since

for high frequencies it is a low impedance path from the base of Q_1 to ground, which tends to increase the loop gain of the circuit. Finally C_3 is a Miller effect capacitor used to control the output rise time.

Table 6-2 tabulates component values for a driver of this configuration that has been used successfully for reading 18-bit words in an LSM constructed of Lockheed 80-07 cores. In the design it was desired to limit the power supply requirements to -12v and +6v. Thus, ground was used for $-E_3$ and E_4; and in order to allow for the back voltage produced by the cores, it was necessary to use some other scheme than clamping the base of Q_2 to $-E_3$. There are at least two alternatives - either replacing D_3 by a reference diode or making R_3 large enough to prevent Q_2 from saturating. The latter course was chosen and R_3 and R_5 were selected to give an output current of greater than 650 ma when h_{FE2} is greater than 20. For transistors with higher gains, the output current will increase, and the base voltage of Q_2 will become more positive which increases the possibility of Q_2 saturating as the cores switch. However, as previously observed, some degree of saturation is permissible when reading if the read current is sufficiently great. Diode D_3 was used (and returned to

Table 6-2

Components and Values used with circuit of Fig. 6-14 to meet the following requirements:

(1) output current to be greater than 650 ma

(2) duration of output to be approximately 10 μ sec

(3) rise time to be approximately 0.15 μ sec

(4) available power supply voltages of -12v and +6v

(5) input to be a negative going 12v transition

Component	Value	Comment
Q_1, Q_2	2N3704	
D_1, D_2, D_3	1N456	
R_1	1.2 K	10%, 1/4 W
R_2	15 K	10%, 1/4 W
R_3	220 ohms	10%, 3W
R_4	8.2 K	10%, 1/4W
R_5	10 ohms	10%, 1W
C_1	0.001 μf	
C_2	50 pf	
C_3	390 pf	
E_1	+6v	
$-E_2$	-12v	
$-E_3$, E_4	ground	

ground) to prevent deep saturation with transistors of exceptionally high gain. The components listed also give a 10 μ sec output pulse with a negative-going, 12v input transition and an output rise time of approximately 0.15 μ sec.

It must be noted that if this circuit is to be used in an application where there is both an upper limit and a lower limit on the output current, it will be necessary to clamp the base of Q_2 at a well regulated potential when Q_2 is conducting.

6.4 Drive Line Terminations [14]

In large and/or high speed memories the drive lines tend to take on the properties of a transmission line. That is, if they are not properly terminated, reflected currents may occur which will adversely affect the current tolerances as well as contribute to noise.

In small linear select memories the drive lines can be kept very short and no problem will arise by returning the drive line to ground or some dc level with no terminations. Similarly in large memories with cycle times of longer than 5 μ sec the terminations are not critical.

For large high speed memories, the drive line termination schemes shown in Fig. 6-15 and Fig. 6-16 have been used. The configuration in Fig. 6-15 is known as the near end shunt termination; and the one in Fig. 6-16 is termed the far end series termination which is the superior of the two. when very high speeds are required.

The terminating resistors would typically be on the order of 50 to 200 ohms or the small-signal, high-frequency impedance of the drive wire. In the near-end shunt configuration the current would initially tend to halve between the resistor and the drive line, but in the far-end series situation all of the driver's output is delivered to the load. However, the far-end termination requires power supplies of much greater voltage to overcome the voltage drop that will occur across the series resistor.

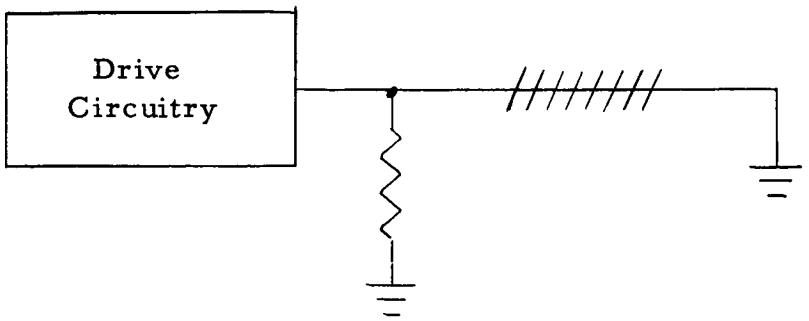


Fig. 6-15 near-end shunt termination

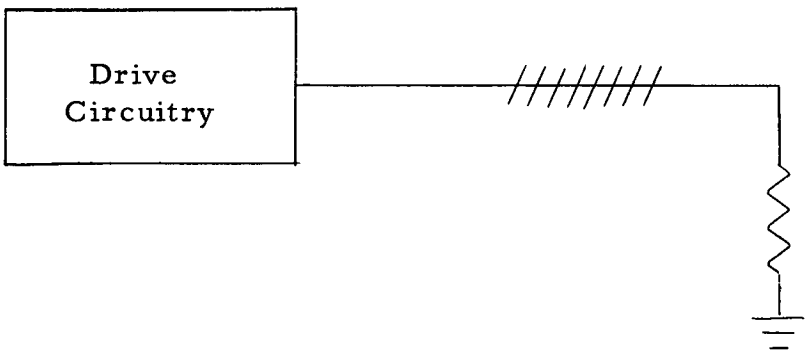


Fig. 6-16 far-end series termination

6.5 References for Chapter 6

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CHAPTER 7

SENSE AMPLIFIERS

7.1 Introduction

Sense amplifiers suitable for use with fairly large and high speed core memories are commercially available in descrete component form as well as in integrated circuit form. Prices appear to range from $25 to $150 apiece, and nearly all are designed for use with CCM's in that they allow bipolar input signals and have provision for strobing. The output signals and strobe input requirements are generally compatible with line of logic circuitry produced by the manufacturer of a given amplifier. Furthermore provision is usually made so that the amplifier gain and threshold are adjustable; this allows a particular amplifier to be used with a variety of cores and core arrays.

While the cost per unit appears rather high, notice that if sense amplifiers costing $100 each are used with a 1000 word memory, the cost per bit of stored data is only ten cents. It is therefore apparent that commercial sense amplifiers exist at a reasonable cost for memories of 100 words or more.

The integrated circuit sense amplifiers are generally less expensive than their descrete component counterparts; and because the integrated models are relatively new to the market, their prices are on a downward trend. Further advantages of the integrated sense amplifiers are that they are compatible with various lines of integrated logic circuitry and that they are physically small.

For small memories, especially low speed ones, the design constraints on the sense amplifiers are relatively relaxed, and often times a fairly inexpensive unit may be designed.

The following sections of this chapter review the considerations which must go into the design of a sense amplifier, and examples of existing sense amplifiers are presented.

7.2 Design Considerations

7.2.1 Components of the Input Signal

The voltage difference across the terminals of the sense winding is the input to the sense amplifier, and the function of the sense amplifier is to determine when any core threaded by the sense winding makes a one to zero transition. Thus, the presence or absence of a one voltage signal (UV_1 or DV_1) from the addressed

core at read time is the input information; if this signal is present, the amplifier is to produce a suitable output to acknowledge that a one was read. This signal, however, will be masked by noise and interference; at best the noise will consist only of the relatively small voltage produced by reading a zero, (DV_Z). The zero voltage and the one voltage from a given core will always be of the same polarity; but when a cancelling sense winding is used, signals from two different cores may be of opposite polarities. Other effects which interfere with the output from the addressed core are:

(1) The noise due to partially selected cores during the read cycle in the CCM.

(2) The common mode voltage excursions of the entire sense winding due to stray capacitive coupling to ground and/or other memory windings.

(3) The large signals that are likely to be developed during the write portion of the memory cycle.

(4) The continual reading and generation of unipolarity signals will cause a dc level in the voltage waveform seen across the terminals of the sense winding.

In small and/or low speed memories these effects can be made minimal.

7.2.2 Electronic Functions to be Performed

In general there are three functions to be performed within the sense amplifier: they are:

(a) Amplification of the input signal,

(b) Discrimination between signal and noise,

(c) Shaping of the discriminated output to a signal compatible with the external logic circuitry.

Each of these cases will be discussed in turn recognizing that there will probably be overlapping between steps.

(a) AMPLIFICATION

Amplification of the input signal is usually necessary before discrimination can be conveniently made. Points which should be considered are:

(1) The gain must be sufficient to amplify the sense line signal to voltage and/or current levels that lend themselves to easy discrimination. If the core output is to be amplified

linearly, then the gain is adjusted so that the amplifier does not saturate for an input swing corresponding to the maximum UV_1 expected. However, much larger inputs - particularly in large high speed memories - may occur during the write portion of the memory cycle which may saturate and temporarily disable the amplifier. If provision is made to amplify this write noise linearly, then the output swing for reading a one will be minimal. To give maximum output swing for reading a one it may be necessary to use limiting circuitry somewhere in the amplifier to prevent saturation while writing[1]; or, as an alternative at the sacrifice of speed, the memory timing can be adjusted so that the read portion of the cycle does not occur until all transient effects of the write portion have disappeared. Finally the gain should be made stable over the operating temperature range and with component aging.

(2) The upper corner of the <u>frequency response</u> characteristic should be high enough to allow reasonably undistorted passage of a UV_1. A lower limit on the upper corner may be estimated from knowledge of T_S and/or T_P for the core being used. The one output voltage may be approximated by a half $(\text{sine})^2$ pulse, that is

$$UV_1 \approx (\text{peak value of } UV_1)\ \text{SIN}^2\left(\frac{\pi}{T_s}\, t\right)$$

for

$$T_0 \leq t \leq T_S \qquad \text{and}$$

$$UV_1 = 0$$

for all other values of t^1 (t = time). The frequency spectrum of this waveform is quite close to zero for frequencies greater than $2/T_S{}^2$, and $2/T_S$ may be taken as the lower limit in question. Since T_P is generally less than $\frac{1}{2}T_S$, using $1/T_P$ for the lower limit would give a higher and more conservative estimate. Recalling that a typical value of T_S is one microsecond, it is observed that a typical sense amplifier would pass frequencies up to at least two megacycles per second.

Because the frequency components of a UV_1 and the noise generated by partially selected cores and by reading a zero are different it is possible to design the frequency characteristic to aid in the discrimination process. In particular recall that the peak value of noise due to non-switched cores occurs during the rise of the drive current pulse and that the peak value of a UV_1 occurs after the current rise. The significant frequency compo-

nents which make up the noise are therefore higher than those which make up a UV_1. But from the usual way that I_D/I_M is defined (refer to Section 4.2), a DV_Z may have approximately one-half the time duration of a UV_1; and the fundamental frequency component of the noise waveform may therefore be as low as approximately twice that of the one output voltage. As a result, discrimination entirely on a frequency basis would be rather hard to achieve[1]. But an improvement in the signal-to-noise ratio at the output of the amplifier would result if the upper corner of the frequency characteristic were such as to not amplify the noise with as much gain as the significant frequency components of a UV_1. Notice that by so doing it is likely that some distortion would result in the amplified UV_1.

(3) The time delay through the amplifier must be taken into consideration, when strobing will be used to aid the discrimination process. The delay time of two amplifiers of the same design will vary slightly because of differences in components. When the timing of the strobe signal is critical as in large memories, it will be necessary to ensure that the delays of all of the sense amplifiers are as uniform as possible.

(4) The sense winding behaves as a transmission line, and the input impedance of the amplifier should match the characteristic impedance of the winding. This impedance is usually in the range of 150 to 250 ohms[3], and manufacturers usually recommend an impedance to terminate the sense windings of commercial bit planes. In lieu of such information it may be necessary to determine a suitable termination experimentally.

(5) The effects of the common-mode component of the signal may be eliminated if the amplifier has a high degree of common-mode rejection, that is, if it amplifies only the voltage difference across the terminals of the sense winding. This is normally achieved by either coupling the sense winding to the amplifier by means of an isolation transformer - which is convenient for matching the sense line impedance to the amplifier with the possibility of providing voltage gain as well - or by using a differential amplifier for the first stage.

(6) In cases where a cancelling sense winding is used it is usually necessary that full-wave rectification be performed within the amplifier so that unipolarity signals emerge from the output. This is normally performed before the discrimination

stage since a decision element can be best designed to operate on unipolarity signals[1]. If the rectification stage used causes a voltage drop in the signals, the stage is best placed after initial amplification stages. Notice that the use of a differential stage at the input will provide gain as well as phase-splitting; the two single ended outputs which are available may be ORed together at a later stage which completes the rectification process.

(7) The discrimination will usually be performed by comparing the amplifier output (at strobe time) with a fixed d.c. voltage level. If the amplifier is a.c. coupled, it may be necessary to allow the reactive coupling elements to return to their quiescent states between successive inputs to prevent a d.c. level shift at the output of the amplifier, which would be detrimental to the decision process. For high speed memories it may be necessary to restore the d.c. levels artificially, by means of a switch, prior to every read operation[1, 3]. With amplifiers that are entirely direct coupled the problem does not arise since there are no energy storage devices.

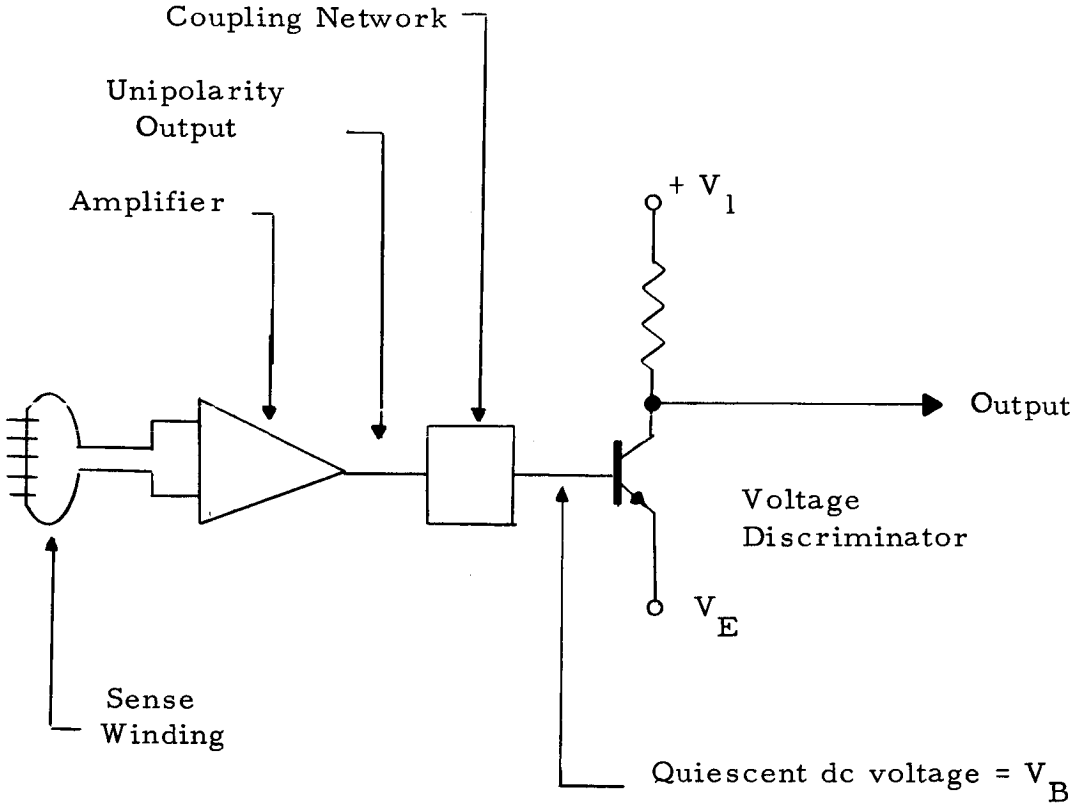
(b) DISCRIMINATION

Discrimination between the signal and noise is the most important function of the sense amplifier, and the form of the

the discriminating circuit will depend primarily upon the inputs that will be presented to it. Basically an amplitude discrimination is made, and often times it is made with the aid of a strobe signal.

To illustrate the considerations involved, Fig. 7-1 shows a simple voltage discriminator using a single transistor coupled to the output of amplifier whose input is from a sense winding. It is assumed that the amplifier and coupling network process the input signals so that unipolarity signals are presented to the discriminator. The coupling network provides a dc path from the supply voltages so that the base of the transistor shown is normally maintained at a voltage V_B which is less positive than the emitter voltage V_E. The transistor is cut off, and the output of the coupling network must change positively by an amount $V_E - V_B + V_{BE}$, where V_{BE} is the base-to-emitter voltage which occurs when the junction is forward biased, in order to cause the transistor to conduct. The voltage change at the collector indicates that the threshold has been exceeded, and it is noted that further voltage amplification is thereby provided

It is important to note that the threshold, as with the switching threshold of a core, will not be precisely defined. There will probably be a region of inputs which will be sufficient to cause



Threshold = $V_E - V_B > 0$

Fig. 7-1 A Simple Voltage Discrimination Method

small, ambiguous outputs.

In setting the threshold it is necessary to consider how the sense line inputs have been processed by the amplifier up to the discrimination stage. The threshold must be set low enough to ensure that the minimum possible "one" output voltage from the memory presented to the discriminator will exceed the threshold enough to cause an intelligible output, and it must be set high enough so the noise will not exceed the threshold. Aside from the amplified noise produced by partially selected cores and reading a zero, the common-mode excursion may not be entirely rejected by the amplifier; and it will effectively contribute to the noise. Also if the discriminator is ac coupled to the amplifier, then, as previously explained, V_B will be a function of the transient response of the network.

The discriminator may be strobed either at the input or at the output to enhance the signal to noise ratio. If strobing takes place at the input, then an AND gate (or transmission gate) is included in the coupling network; and it is arranged so that no input signal is allowed to pass to the discriminator until the strobe signal is present. Care must be taken in the design to ensure that the strobe signal does not cause an undesirable transient to be

superimposed on the signal. If, on the other hand, strobing takes place at the output, the output is fed directly to an AND gate which is enabled by the strobe signal. If the signal into the discriminator exceeds the threshold during the strobe period, an output will occur.

A third method of strobing is to change the threshold from an exceedingly high one, which is normally present, to the one to be used for the actual discrimination. In Fig. 7-1 this could be accomplished by switching V_E from an open circuit (infinite threshold) to the required potential for discrimination.

Finally it is observed that the strobing function could be placed elsewhere in the amplifier by use of a suitable transmission gate.

The exact timing of the strobe signal will be determined by the particular memory under consideration. In memories where the noise is low it will probably be sufficient to have the strobe signal present at the same time that the full read current is applied. In large, high-speed memories, it will be necessary to delay the presence of the strobe signal until the noise has essentially died away as indicated by Fig. 5-6. In

either case it is noted that the strobe will pass a signal that is no longer in time than T_S. The resultant output may be too narrow to act as a reliable logic signal, and it will require shaping.

(c) SHAPING

The output of the sense amplifier must be shaped so that it will reliably operate the logic circuitry that it is to drive. For operating low speed logic it will probably be necessary to provide a pulse considerably wider than that produced from the memory. This might be achieved by use of a monostable multivibrator, blocking oscillator, or by use of positive feedback in the amplifier itself. Alternatively, the logic circuitry might be modified so that it will operate from a narrow amplifier output.

7.3 Sense Amplifier Examples

7.3.1 A Low Cost Sense Amplifier For A Small Low Speed LSM

The sense amplifier shown in Fig. 7-2, which was designed by David Vlack of the Digital Systems Laboratory at Case Institute of Technology, is intended for use in a small, low-speed LSM. In particular the speed requirements of the memory for which it was designed allowed several milliseconds between successive write and read operations. The memory

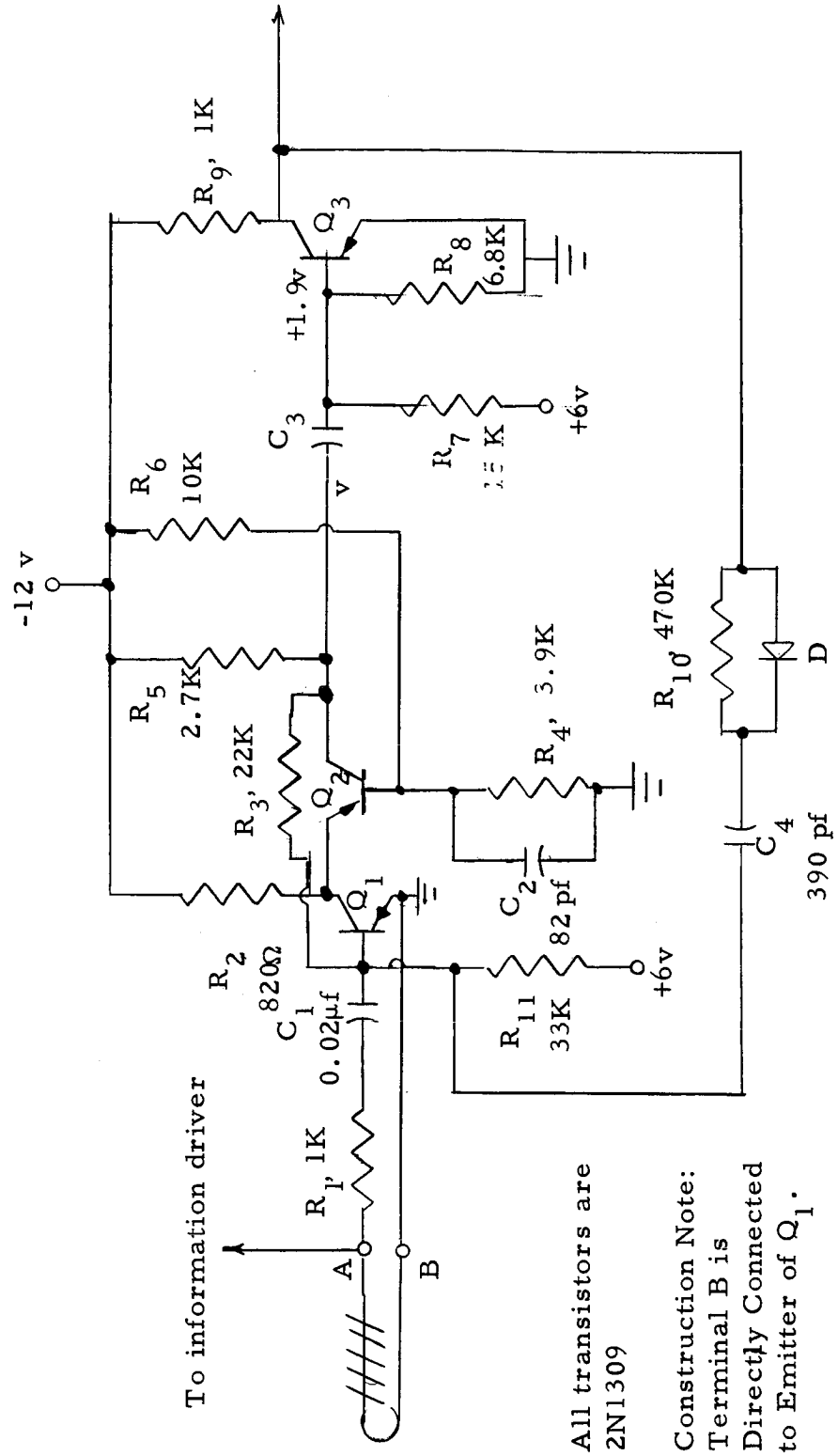


Fig. 7-2: A Low Cost Sense Amplifier For a Small, Low Speed LSM.

output during read consisted of only positive going UV_1's of peak values greater than 150 mv, with T_S approximately one microsecond, and DV_Z's of less than 40 mv in peak value.

The low speed requirements suggested that the information current driver and the sense amplifier could share the same winding, since there is ample time available for the amplifier to recover from inputs due to writing. Thus input terminal A is common also to the information driver output, and terminal B is connected directly to ground.

The required output of the amplifier is a positive going, 12v pulse of five to ten μ sec in duration to occur only when a one is read.

Transistors Q_1 and Q_2 are arranged to form a d-c coupled amplifier with a negative gain. Negative feedback current through R_3 tends to stabilize the operating points and the gain with respect to temperature variations and aging. The input is ac coupled through R_1 and C_1, and the input signals are voltage amplified with a gain of approximately $-R_3/R_1 = -22$ (since R_3 forms part of the bias network the gain should be adjusted by varying R_1 only). The output of the amplifier is a.c. coupled to

the threshold circuit comprised of Q_3, R_7, and R_8. Q_3 is normally held at approximately + 1.9v by virtue of the voltage divider R_7 and R_8. Thus Q_3 is normally cut off, and a rapid, negative-going, voltage change of magnitude greater than 1.9v at the collector of Q_2, which corresponds to an input greater than 90 mv, is required to cause Q_3 to start to conduct. When Q_3 does start to conduct, positive feedback from its collector through the diode, D, and C_4 (which is initially charged to -12v) to the base of Q_1 adds greatly to the input signal; Q_1 and Q_2 are cut off, and Q_3 is driven into saturation. The collector of Q_3 has then made a -12v to ground transition. The charging current through C_3 keeps Q_3 saturated for close to 10 μ sec. When Q_3 is finally cut off again, the negative-going transition cannot be passed by D, and C_4 charges slowly, with a time constant of approximately C_4R_{10}= 183 μ sec, to its quiescent potential of -12v. If the parallel combination of R_{10} and D were not present, the positive feedback from the trailing edge of the output could cause unwanted oscillations.

Since the time constant associated with changing C_4 to its quiescent value is considerably longer than that associated with the other capacitors, the recovery time is essentially 5 C_4R_{10} or

approximately one millisecond.

7.3.2 Typical Integrated Sense Amplifier[4]

The schematic diagram for the Signetics Corporation's Model SE 504 integrated sense amplifier is presented in Fig. 7-3, and it is typical of many integrated sense amplifiers. It is entirely d.c. coupled and has an upper corner frequency of 3 mc so that it should be suitable for use with high speed memories.

The differential input stage Q_2 and Q_3, biased by the constant current generator Q_1, provides common-mode rejection, amplification of the input, and phase splitting. The two outputs from the collectors of Q_2 and Q_3 are inputs to the current-mode OR gate comprised of Q_4, Q_5 and load resistor R_9. The biasing is arranged so that Q_4 and Q_5 are normally cut off; both emitters are at a potential V_9, which is less positive than the collector supply voltage V_8, supplied externally through pin 9. When the voltage difference across the input terminals, 5 and 10, causes the collector of either Q_2 or Q_3 to become more positive than V_9, either Q_4 or Q_5 will conduct, and a voltage drop will occur across R_9. Transistor Q_6 acts as an AND gate for strobing. The strobe input would normally be held at a potential more negative than V_9,

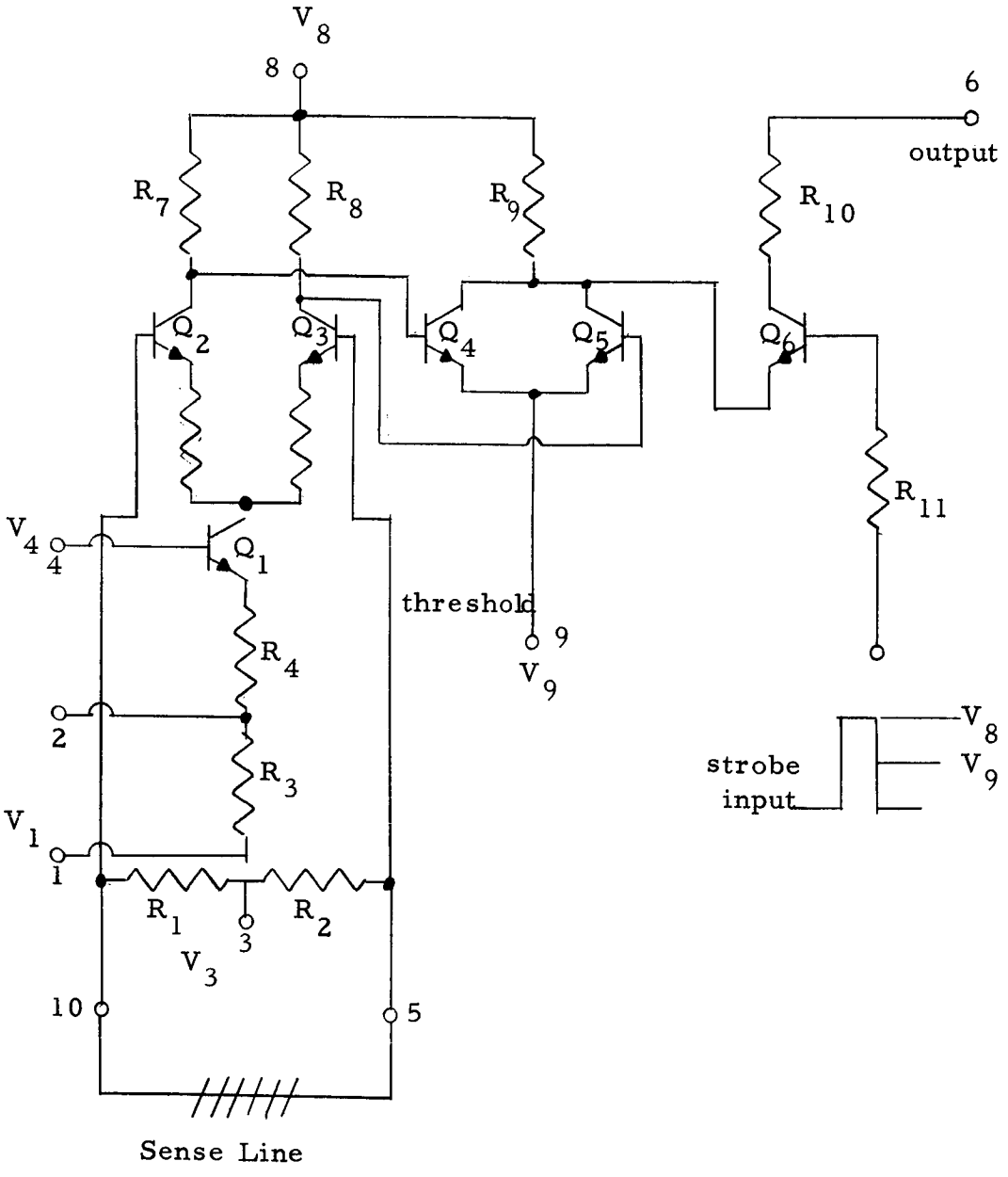


Fig. 7-3 Typical Integrated Circuit Sense Amplifier

so that the transistor is normally cut off. Switching the input to $+V_8$ at strobe time will allow Q_6 to conduct only if either Q_4 or Q_5 is conducting.

7.4 References for Chapter 7

1. Goldstick, G.H., and Klein, E.F., "Design of Memory Sense Amplifiers", IRE Transactions on Electronic Computers, Vol. EC11, April, 1962, pp. 236-253.

2. Reference Data for Radio Engineers, New York: International Telephone and Telegraph Corporation, 4th Edition, p. 1014.

3. Quartly, C.J., Square-Loop Ferrite Circuitry: Storage and Logic Techniques, London: ILIFF Books Ltd. (Englewood Cliffs, N.J.: Prentice Hall, Inc.), 1962 pp. 100-104.

4. "Preliminary Specification for Series SE 500 Gates Sense Amplifier", Signetics Corporation, Sunnyvale, California.

CHAPTER 8

COMMENTS ON CORE MEMORY DECODING LOGIC

8.1 Introduction

The function of the decoding logic is to allow the addressing current pulses to pass through only the line or lines of cores specified by the contents of the address register. Recall that in the LSM only one line of cores is chosen, and the selection of the proper line is based upon the entire contents of the address register as indicated by Fig. 3-12. In the CCM, however, two lines - one in the X direction and one in the Y direction - are selected; and the usual procedure is to have the selection in one dimension be determined by part of the address register and to have selection of the other dimension be determined by the remainder of the register [1, 2].

Thus, the decoding logic in the CCM may be broken into two distinct parts with each part having inputs from a given segment of the address register. In some instances the division of the register may be such that one or more flip-flops will be common to both segments. But with either the LSM or the CCM the decoding logic design reduces to going from a given register (or segment of a register) to selecting the one line corresponding to the state of

that register. There are two conceptually simple methods of doing this, and they are illustrated in Fig. 8-1 and Fig. 8-2.

In Fig 8-1 there is a read-current driver and a write-current driver for every line. The decoding logic, which is entirely combinational and might be a diode matrix, enables only the current drivers for the proper line by means of the AND gates (note that the AND gates would probably be a part of the driver circuitry). Upon receipt of a read or write command, only the selected core will be driven by the corresponding current.

In Fig. 8-2 there is a normally open switch in each line, and common to all switches there is a single read-current driver and a single write-current driver. The decoding logic, which is essentially of the same form as in Fig. 8-1, provides an output which closes only the switch in the selected line. Then upon receipt of a command, drive currents will flow only through the chosen line. For very low speed operation the switches may be mechanical contacts such as inexpensive reed switches, but for higher speeds electronic switches such as transistors would have to be used. A further point to note is that it would be necessary to allow time for the selected switch to close before applying the read or write command.

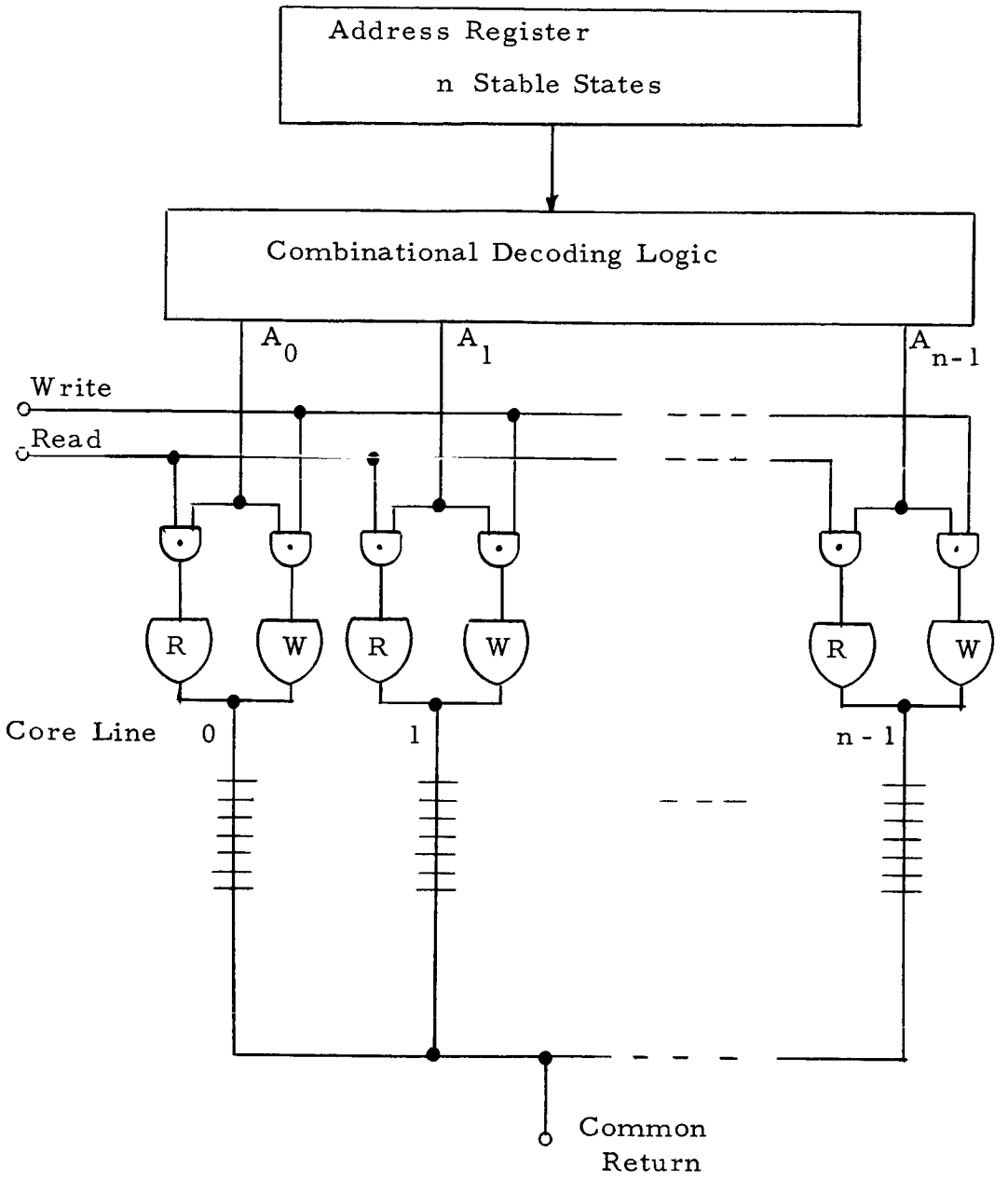


Fig. 8-1 Core Line Selection Using One Read Driver and One Write Driver per Core Line

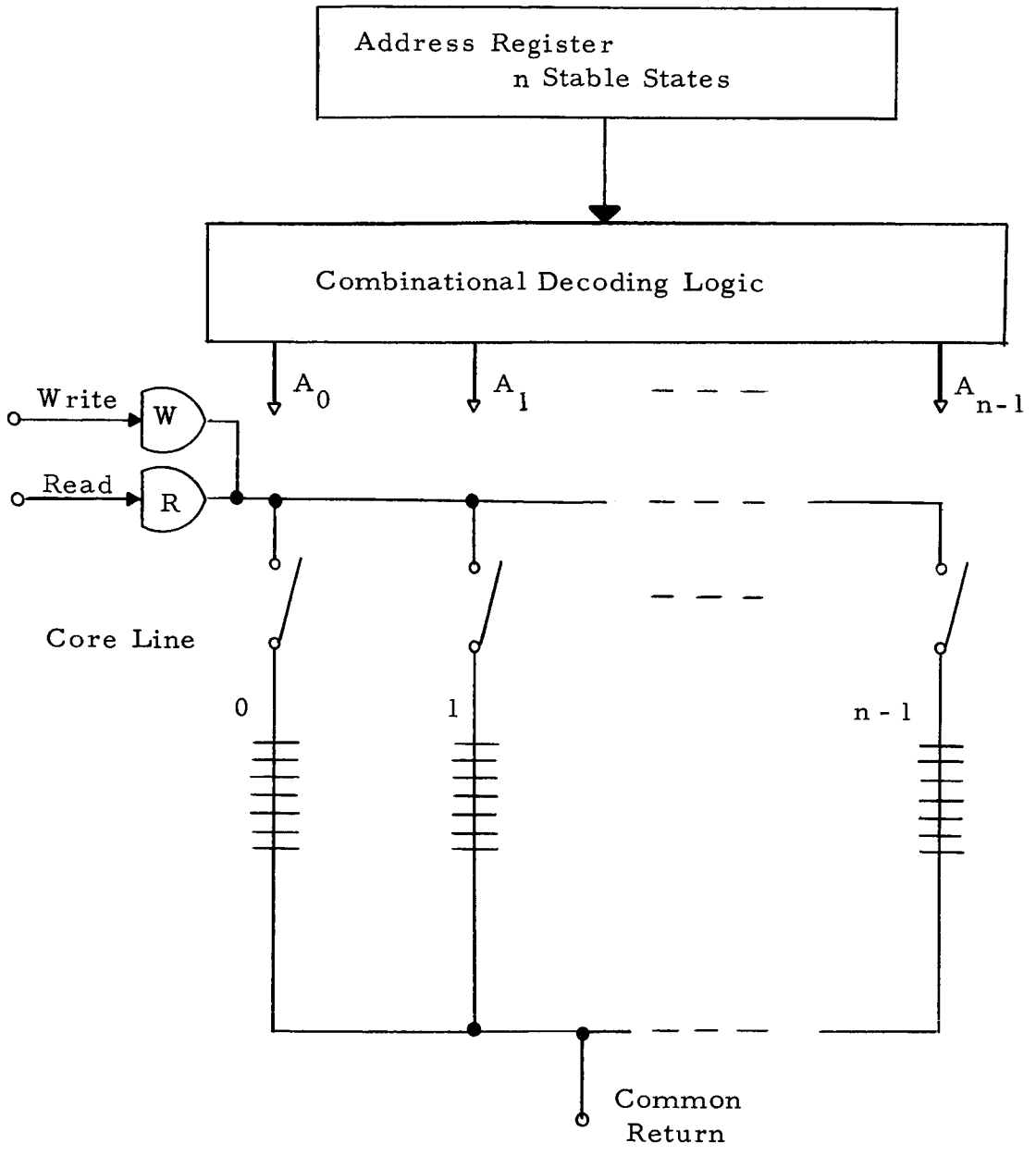


Fig. 8-2 Core Line Selection Using One Switch per Core Line

(n outputs of the decoding logic select the proper normally open switch)

The switches in Fig. 8-2 are shown on the side of the memory that is common to the drivers; but they may, if desired, be placed on the opposite side of the core array. It is pointed out, however, that placing the switches on the opposite side could cause a noise problem because the potential of the unselected lines would then follow the back voltage developed across the driven line. These voltage changes would be coupled to the sense winding(s) by the stray capacitance that exists in the core array[1]; and as the size of the memory increases, the effect will be more and more detrimental to discrimination in the output.

There are two general techniques that have been used to reduce the necessary combinational logic as well as the number of drivers and/or switches required by the above two schemes. These are discussed in the following two sections.

8.2 Decoding Simplifications by Connecting the Core Lines to Form a Matrix

8.2.1 Circuit Forms

Fig. 8-3 illustrates the decoding simplifications that result by connecting the core lines to form a matrix and by using normally open switches on both sides of the memory (note that the

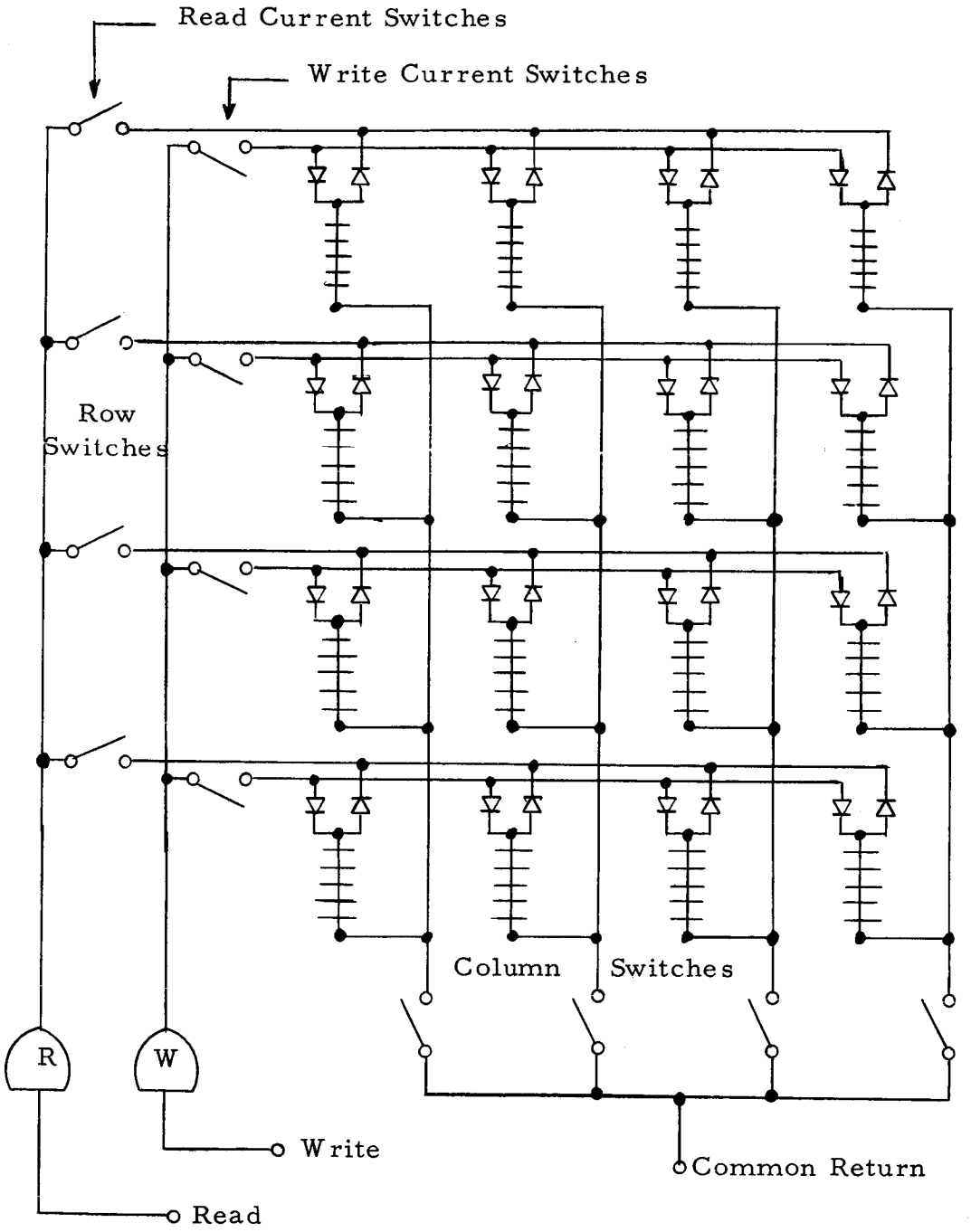


Fig. 8-3 Decoding Simplification with Core Lines Connected in a Matrix

diagram does not show the physical orientation of the lines). To allow read current to flow in a given line, the read-current switch in the row (that is, on the side common to the current drivers) of the core line and the proper column switch (that is, the switch on the side of the memory opposite to the drivers) are both closed. The read-current pulse may then be applied, and the only path for the current is through the desired core line. In a like manner, to apply write current to a given line the write-current switch in the proper row and the proper column switch are closed prior to the write command.

The diodes shown are necessary to ensure that current will flow only in the selected core line, and they also provide isolation between the voltage changes on the driven line and the stray capacitive coupling of the unselected lines - in the selected row - to the sense winding.[1]

In comparison to Fig. 8-2, it is seen that this scheme requires fewer switches, and the combinational logic necessary is reduced from a one out of n selection to a one out of j selection plus a one out of k selection, where j is the number of rows, k is the number of columns, and jk = n. This allows the address register to be divided into two segments in an LSM; and applying

the idea to a CCM, allows the address register to be divided into four segments.

There are several variations on the scheme. Two forms which have appeared in the literature are shown in Fig. 8-4 and Fig. 8-5, and combinations of the ideas may be arrived at.

It is noted and emphasized here that in all of these schemes the switches used for reading must be closed independently of those for writing. In very small memories of less than 50 to 100 words the extra logic circuitry required to do this could cause the price of one of these schemes to be greater than the cost of a system of the one shown in Fig. 8-1 or Fig. 8-2. This is illustrated in the design example in Chapter 9.

In Fig. 8-4[3] there is one read driver per row and one write driver per column (or vise-versa), and there is switch for every row and column. For reading, a read driver and a column switch are selected, and for writing a write driver and a row switch are selected. The decoding logic is the same as required in Fig. 8-3, but some extra gating will be required to prevent simultaneously closing a column switch and a row switch. Fewer switches are required than in Fig. 8-3 at the expense of more drivers. However, the cost of a driver might not be too much

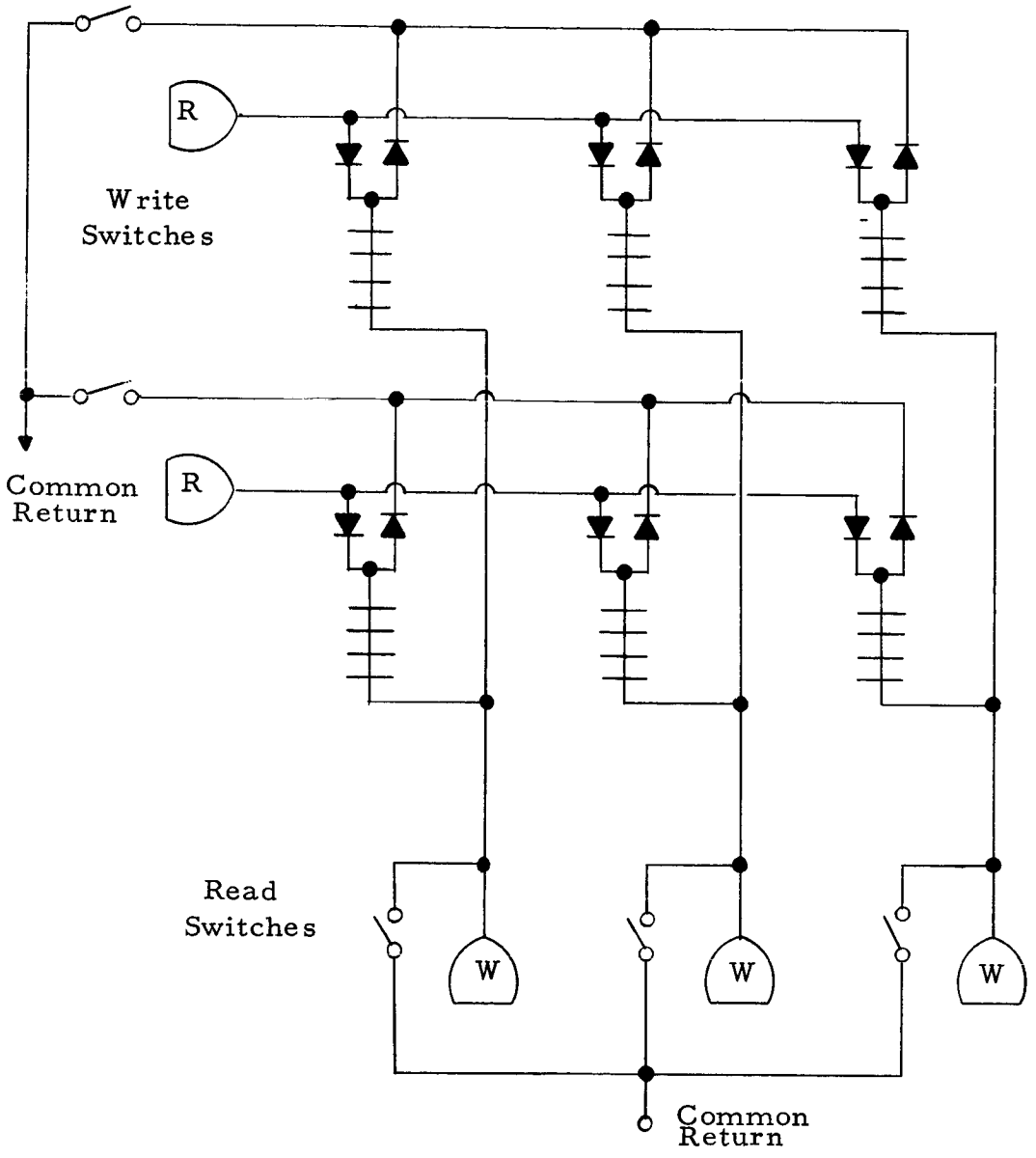


Fig. 8-4 Decoding Using Switches and Drivers on Both Sides of Core Line Array

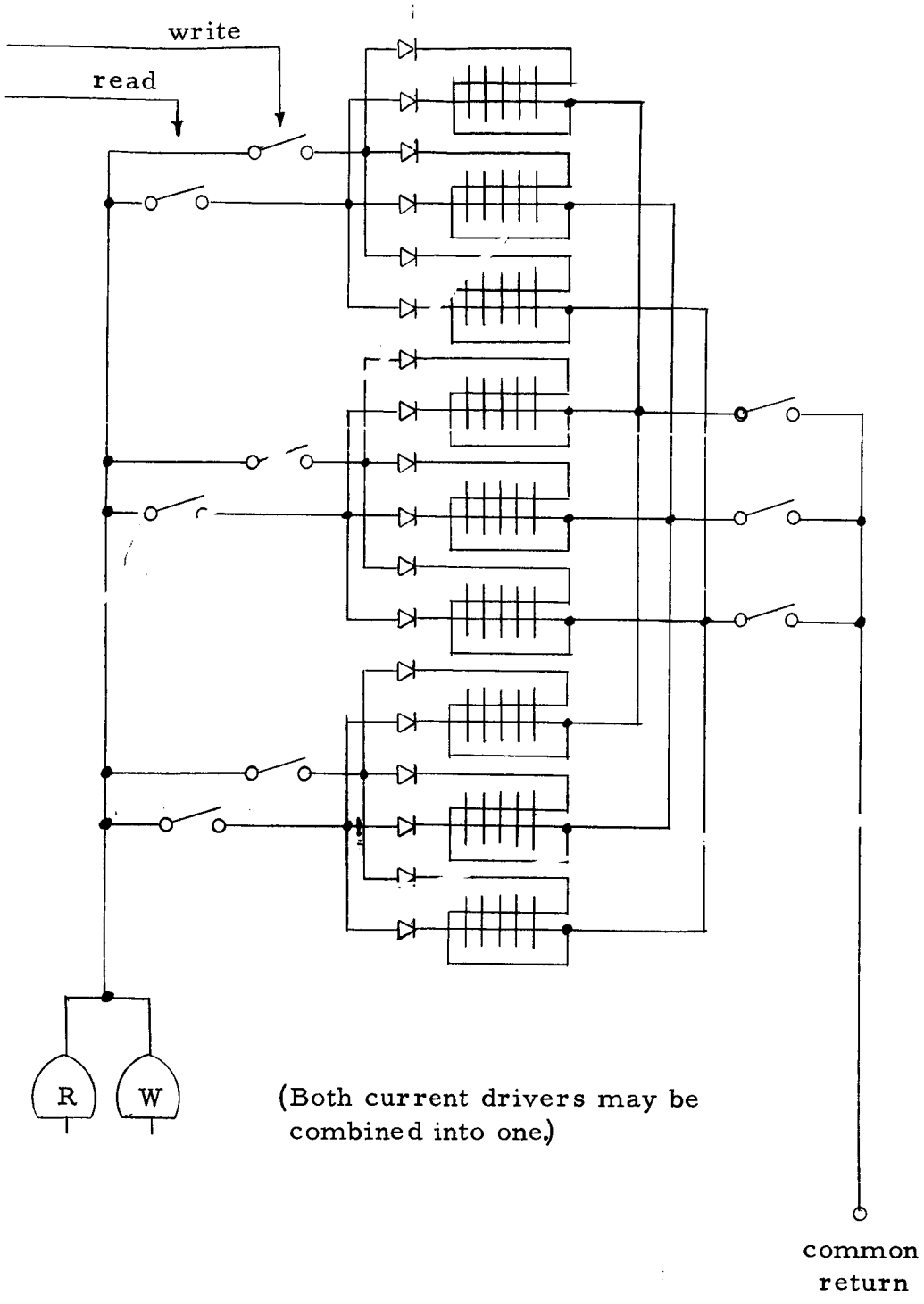


Fig. 8-5: Decoding Simpliciation by Using Extra Drive Wires

more than that of a transistor switch, and all of the switches used in this scheme are required to pass current in one direction only which implies a cost savings (as far as transistor switches are concerned) over the required bidirectional column switches in Fig. 8-3. Note also that all of the current drivers produce currents of the same polarity with respect to the power supplies; read and write currents are merely passed through the cores in opposing directions.

In Fig. 8-5[1, 4, 5] two wires, threading the cores in opposite directions, are used per core line. The circuitry is otherwise the same as in Fig. 8-3 except that only bidirectional switches are required, which tends to compensate for the price of the extra wiring.

It is emphasized that the disadvantage of all of the matrix connections is that separate switches are required for reading and writing. Extra logic will be required to close only the proper switches for the function to be performed, and it is usually necessary to enable the switches prior to application of the drive currents which implies longer cycle times and extra timing circuitry.

8.2.2 Transistor Switches

The design of transistor switches for use in decoding is closely related to the design of the current drivers. There are two situations to be considered: switches between the current driver and the cores and switches on the opposite side of the memory from the driver.

A transistor in a common base configuration with the cores in the collector circuit is suitable for the first case. The circuitry is indicated in Fig. 8-6, where two switches with a core line in the collector circuits and with both emitters common to the output of a current pulse generator are shown. The switches are held off by maintaining the base voltages at $-V_1$ volts, the potential from which the current is derived. To turn a switch on its base voltage is switched to V_2 to bias the transistor in the active region. That is, $-V_1 < V_2 < V_3$, where V_3 is the common return potential of the core lines. If the current at the driver output is I_D, the current delivered to the cores is $\frac{h_{FE}}{1+h_{FE}} I_D$, where h_{FE} is the common-emitter current gain of the transistor. This relationship will hold so long as the transistor does not become saturated, and in order to faithfully transmit the current pulse, V_2 should be chosen so that the back voltage from the cores

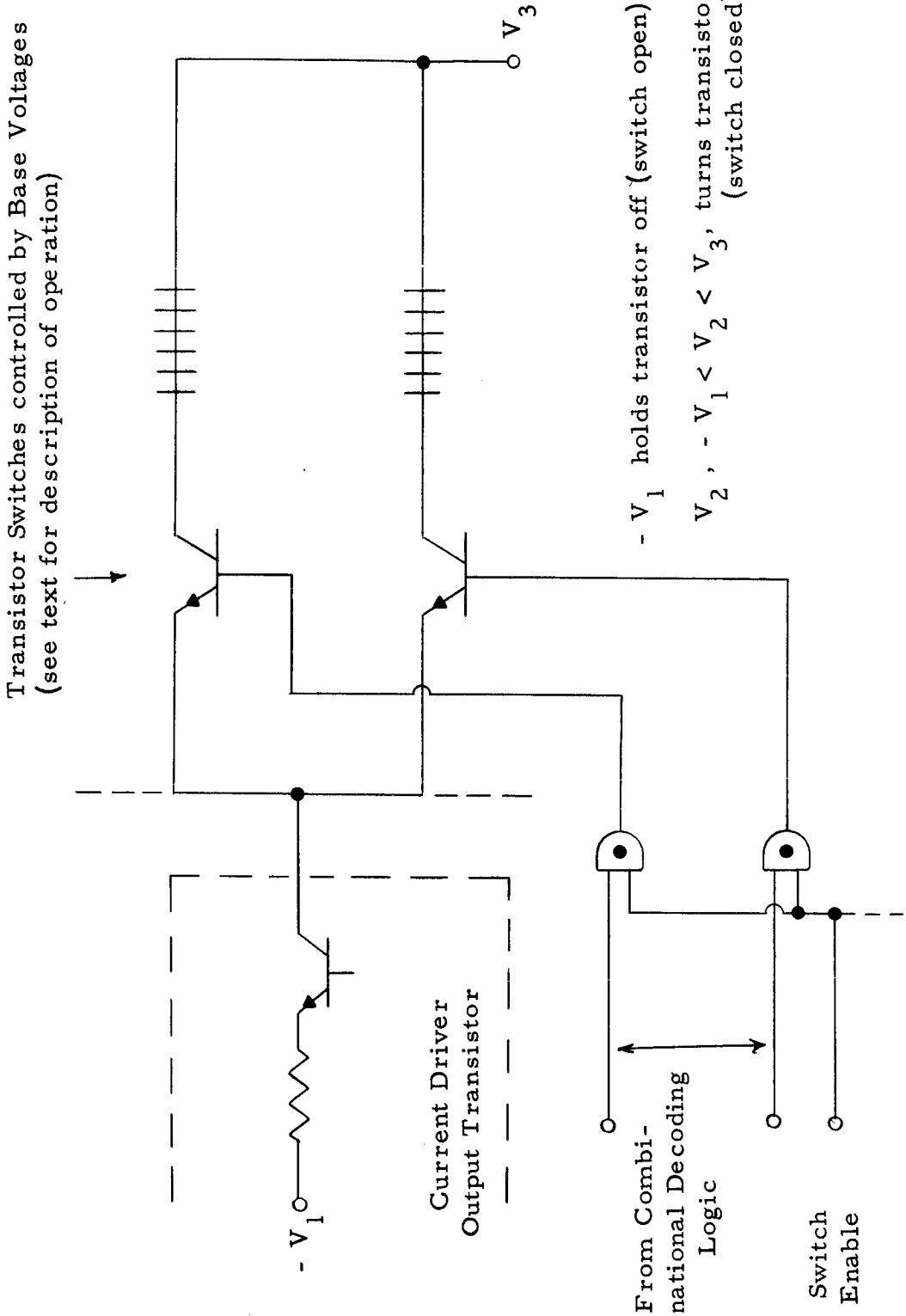


Fig. 8-6 Transistor Switches between Driver Output and Core Line

does not cause saturation. Variations in h_{FE} between transistors will, of course, adversely effect the current tolerances and should be taken into account in the design. By allowing the switches to absorb the back voltage, the transistor in the current driver can be allowed to saturate or nearly saturate and still produce an output that is independent of the core voltage. The AND gates shown require a second transistor (and perhaps more) to control the base of the switch and to provide enough current gain to allow sufficient base current to flow to hold the switch on. The AND function is required to turn the transistor on only at the proper time by the switch enable line. Thus, the net cost of this switch would be close to the cost of a driver itself which would require approximately the same component count.

If, as in low speed writing, the shape of the current pulse is not important, a saturated transistor might be used between the core line and the driver. The addition to or the subtraction from the core line current due to the base current - depending upon whether the cores are connected to the emitter or the collector - should be taken into account in the design.

A third possibility is to use a transistor controlled by a pulse transformer, as in Fig. 6-12, (with R_6 removed and

replaced by the driver). This has the advantage that - like a mechanical contact - the collector and the emitter may be at any potential relative to ground, and it has the further advantage that the controlling base current does not effect the output current of the core driver.

In both of the above cases - as with the first case - additional transistors and components will have to be used to provide an AND function and gain.

Perhaps the most convenient configuration for switches on the opposite side of the memory from the driver, is a saturated transistor with the cores connected to the collector as illustrated in Fig. 8-7. A switch is enabled merely by providing ample base current to saturate the transistor prior to application of the drive current, and a switch is held off by reverse biasing the base-emitter junction. Once again a special AND gate is required to hold the switch off until the "switch enable" signal is present. The voltage across the switch when it is on will be on the order of 0.3 v and can be readily taken into account in the driver design.

Notice that these switches are unidirectional, that is, they allow current to flow in only one direction. To implement the

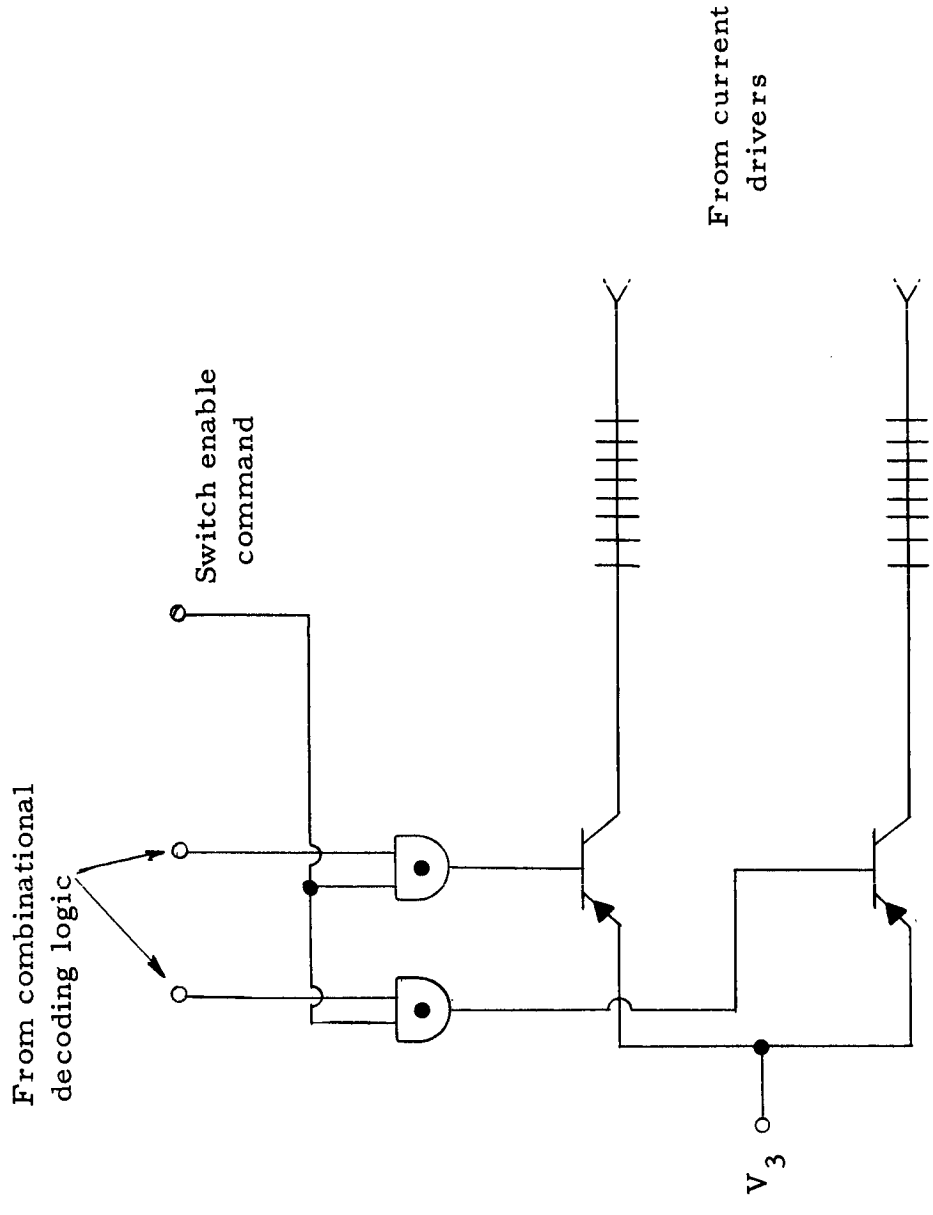


Fig. 8-7 Saturated, Common Emitter Switches on Side of Memory Opposite to Driver

column switches in Fig. 8-3, two unidirectional transistors are required or perhaps a bidirectional transistor could be used[1]. Clearly transistors of the right construction (NPN or PNP) must be chosen for each application.

8.3 Decoding with Switch Core Matrices

It has been found and qualitatively verified in Section 2.2.7 that when a square-loop core with a low impedance load connected to its output winding is switched by a current pulse, a reasonably square current pulse will flow in the output circuit. Many memories have been built using large (in comparison to memory cores) square-loop switch cores (either ferrite or ultra-thin metalic tape) arranged in a matrix to provide a level of decoding logic as well as to transmit bipolar current pulses to the memory cores.[2]

Several techniques have been used, but the one most commonly used in small to medium sized memories is the coincident current scheme shown in Fig. 8-8[6]. Each switch core's output winding is a memory drive line, and when a switch core changes states, current will flow in the associated core line. However, recall from Section 2.2.7 that sufficient current must be

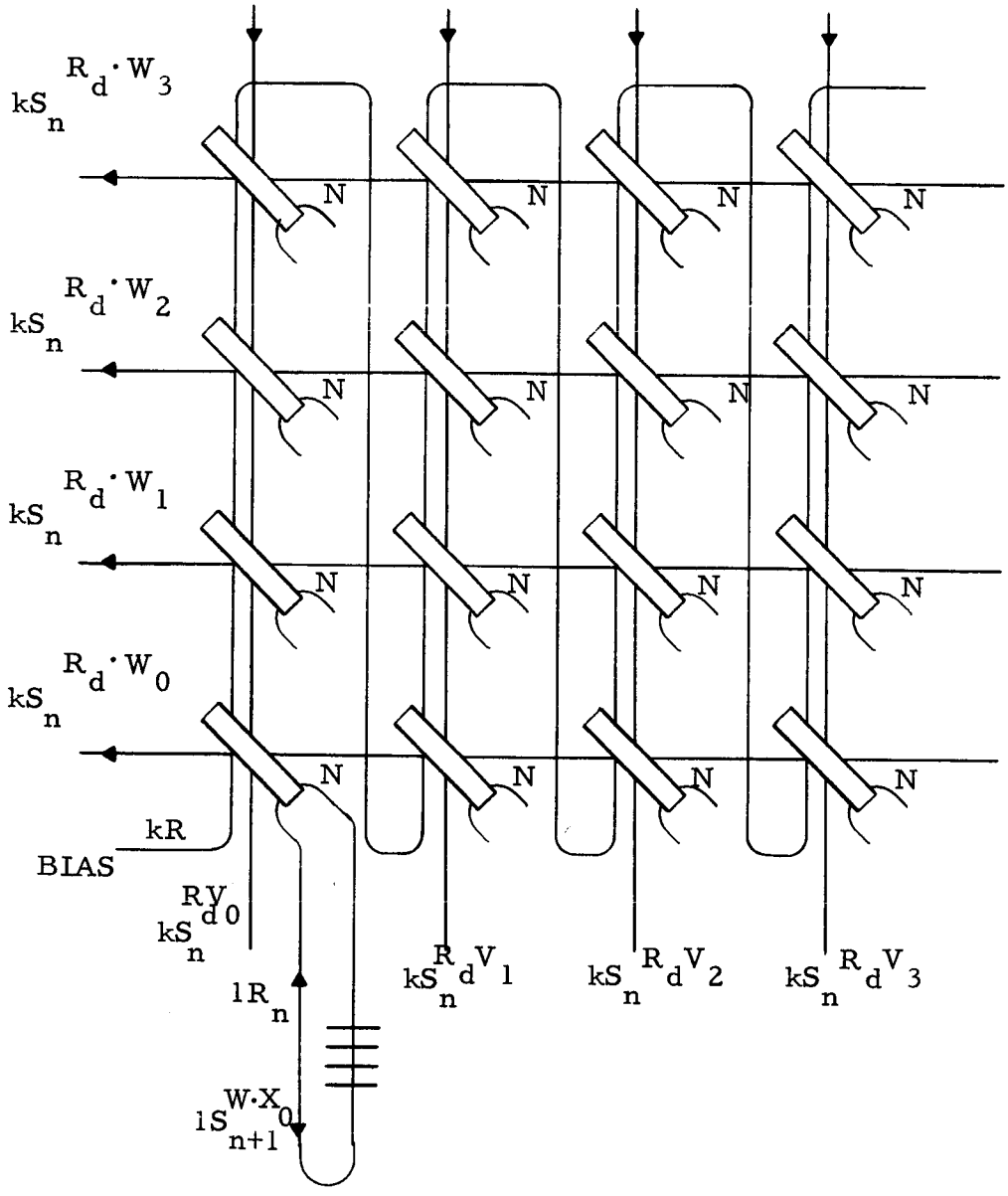


Fig. 8-8
Matrix of Switch Cores to Provide

a Level of Decoding Logic

supplied to the switch core to overcome the switching threshold as well as to overcome the back mmf of the load current. The coincidence of two currents less than the switching threshold is generally not sufficient to switch the core at a rate that will allow the proper current to flow through the memory. To give the necessary overdrive, all of the switch cores are initially in the zero state, and they are heavily biased in the reset direction by the current kR. Then to provide read current at time n to a particular memory line, the corresponding switch core is switched to the one state by the coincidence of the two currents $KS_n^{R_d \cdot U_i}$ and $KS_n^{R_d \cdot V_j}$ at the intersection of column U_i and row V_j. The net current applied to an unselected core in the row or column is zero; whereas, the net current applied to the selected switch core is KS_n. The constant, K, may be much greater than unity, and it is selected to allow the proper current to flow in the memory cores. When the selection currents are removed, the selected core returns to the zero state, by virtue of the bias current, causing current to flow in the write direction in the memory core line. Since the bias current is of the same amplitude as the partial selection currents, the write current output will be of the same amplitude as the read current output. Thus, from unidirectional current drivers, this configuration provides bipolar

currents to the memory for reading and writing, and the coincident current selection of the switch cores simplifies the decoding logic. Notice that after reading, the selection currents must be maintained until it is desired to write; or, alternatively, if the information to be written will not be available for a long time after reading, the selection currents may be relaxed immediately after reading - causing all ones to be written - and applied again later when the data is available.

Several variations of the idea of decoding and driving through matrices of switch cores have been proposed and/or used[2], and Reference 6 reviews those methods which have proved most practical. The use of the idea dates back to the early days of core memories (prior to 1955) to minimize the required number of current drivers which utilized relatively expensive, high-current vacuum tubes[2]. With the advent of today's fairly low cost, high current, Silicon switching transistors, which may be used in switches as well as drivers, this advantage is not as great.

A clear disadvantage is that the small flux changes which occur in the partially selected cores will induce small currents in unselected memory core lines which will contribute to system noise; in an LSM the contribution might be sufficient to

warrant the use of a cancelling sense winding[1] with the implication of a more expensive sense amplifier and increased wiring costs.

The design of the switch core matrices is closely related to the design of magnetic core logic circuitry and shift registers. Design and analysis steps are well documented in the literature in such references as 3, 6, 7, 8, and 9. Important results of the design procedures are:

(1) It is oftentimes necessary that the output winding make several turns around the switch core so that ample voltage is induced to overcome the back voltage from the memory core line.

(2) The mmf which must be applied to the switch core will be considerably greater than that required to drive a memory core.

(3) The load presented to the switch core is quite variable because the number of memory cores that will be switched is variable. Series resistance - on the order of two ohms - is usually added to the core line to make the load more stable and to provide regulation of the current. The wire resistance of the core line itself must be carefully considered in determining the resistance, and in some cases the wire resistance alone is sufficient[6]. The length of the memory drive lines must be well controlled in the construc-

tion process, to give the desired impedance in each line. A large percentage of the switch core's output is used to maintain a nearly constant voltage across this resistance.

(4) The required input current tolerances to the switch cores will normally be tighter than those required by the memory core array[3].

These results point out further disadvantages of the system.

(1) The cost of wiring will be rather high since multi-turn windings will be required.

(2) To provide the large mmf's required, either multi-turn windings must be used for the inputs or higher priced transistors with greater current switching capabilities must be used. For example, if 300 ma of current is required in the memory core line, and if the memory core line makes two turns around a switch core with a coercive force corresponding to 300 ma, then a drive mmf of 900 ma turns is required. A transistor with a rating of 500 ma would probably drive the memory line satisfactorilly; either a transistor with higher ratings is required to drive the switch core or several turns will have to be provided for the switch core inputs.

Thus, while the number of drivers and electronic switches required is reduced, the price paid for the reduction is more expensive wiring plus an increased cost for each individual driver.

8.4 References for Chapter 8

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CHAPTER 9

MAGNETIC-CORE MEMORY DESIGN

9.1 Design Procedure

The purpose of this chapter is to tie together the various points and ideas of the foregoing chapters by presenting a procedure which may be followed in the design of a core memory. The object of this procedure--as is the object of most design procedures--is to allow the designer to at least arrive at a first approximation of a working design with a minimum of experimental work and pure invention in the laboratory.

The procedure starts with the assumption that a magnetic-core memory will provide a good solution to the problem at hand. If it is not clear at first what type of memory will yield the best solution, the design procedure may be followed through to give an indication of how suitable a core memory would be.. While the steps in the procedure will be general enough to allow the design of large memories, the details and emphasis will be directed towards the problems of small memories.

The flow diagram in Fig. 9-1 is used to illustrate the steps to be taken and the interaction between these steps. In each block, with the exception of the one indicating the problem statement, decisions are to be made. These decisions will be based

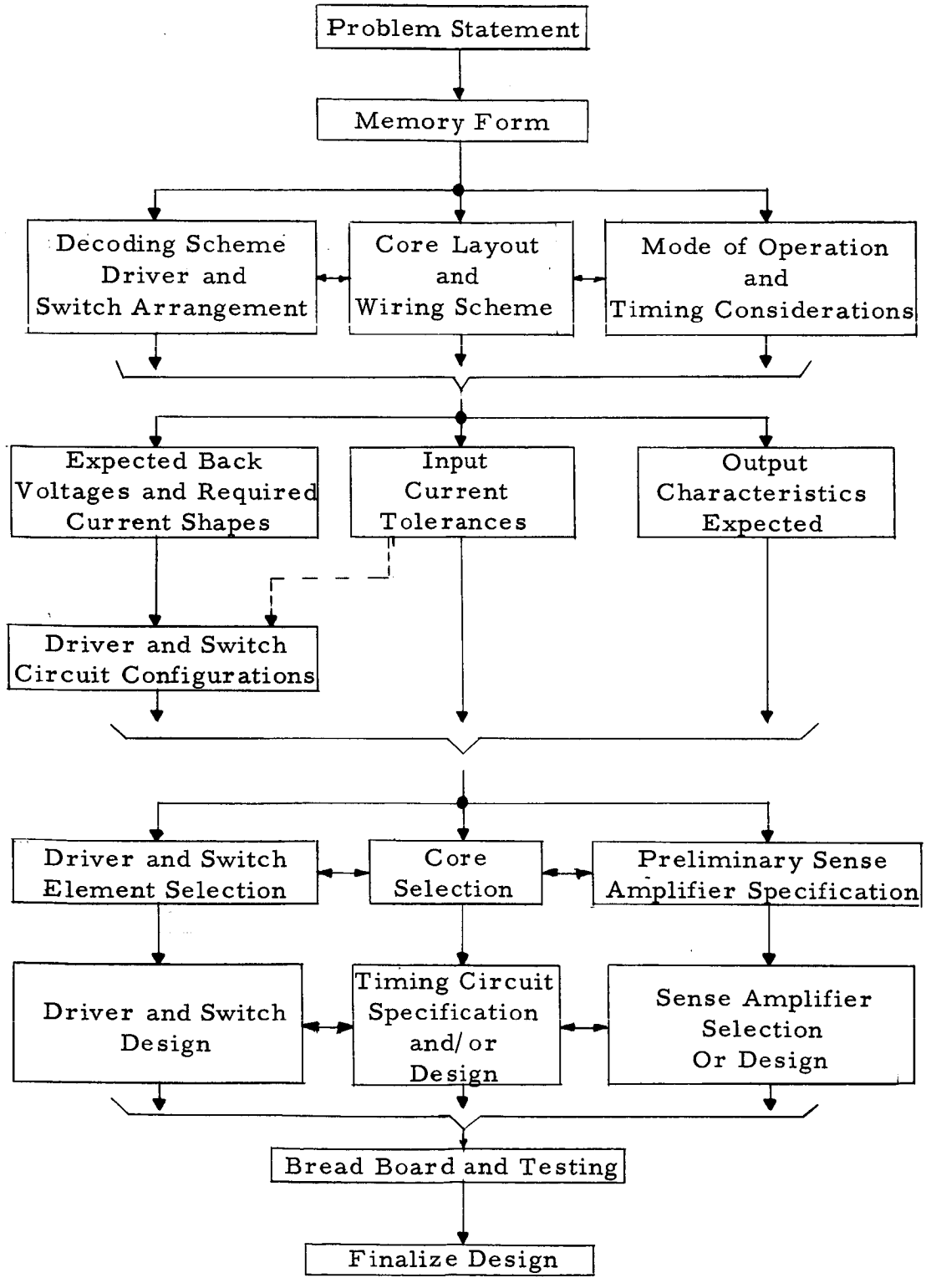


Fig. 9-1: Flow Diagram of Memory Design Steps

upon prior decisions, and after each new decision it is expected--but not shown--that the designer will review his prior decisions and modify them as necessary to arrive at a better all around solution. Blocks on the same horizontal level represent substeps--within a general step--which have a good deal of interaction between them and are consequently best taken concurrently.

Step 1--Problem Statement

The following information should be given initially:

1. A concise statement of the purpose that the memory will serve.

2. The required storage capacity in terms of the number of words to be stored and the number of bits per word.

3. The temperature environment in which the memory will operate.

4. The required speed in terms of access time and/or cycle time.

And whenever possible, it is convenient to include:

5. The form in which the address will be encoded.

6. Definition of acceptable input and output logic signals in terms of levels and transitions between levels.

7. Power supply restrictions.

8. Packaging and mechanical considerations such as physical size and weight.

At this point it might be wise to consider commerically available core memory systems. These are available with word capacities in the range of 256 to 8192 words and with word lengths of up to 40 bits or more. Most of these systems are of the coincident current type, and the total number of words is usually a power of two to give a maximum of decoding efficiency. It is usually required that the address be provided externally as a natural binary number.

Thus, if 200 or more words of storage are required, a commercial memory can probably be found that will fill the problem requirements. However, more memory space than is required might have to be purchased. For example, if 300 words are required, a 512 word memory would be called for. But there are three other possibilities: the problem could be restated so that a 256 word memory would suffice, one could consider purchasing a 256 word memory and designing a small 44 word memory to make up the difference, or a 300 word memory could be designed.

However, if a suitable commercial memory at a reasonable price can be found, the problem can be considered as solved.

Step 2--Determine Memory Form

The problem statement will probably suggest whether a CCM, an LSM, or perhaps some special purpose memory is best suited. In making the choice between a CCM and an LSM recall that the one advantage of the CCM is in the simplification of the decoding logic. The advantages of the LSM are many, and the important ones were listed in Chapter 4. They are briefly repeated here in the light of Chapters 5, 6, and 7.

1. The LSM is simpler and less costly to wire.

2. The LSM requires a less costly sense amplifier because the configuration generates less noise, the outputs are always of the same polarity, and with no upper limit on the read drive a UV_1 can be made very much greater than a DV_Z.

3. The LSM offers looser current tolerances; and hence, less costly drivers.

4. The LSM offers the highest speed and widest temperature range capabilities.

5. The LSM has many times fewer cores on the read drive wires, and as a result, the read current rise time will not be retarded by many partially selected cores.

For small memories these cost savings normally overcome the extra cost of decoding, and an LSM is indicated. Reference 1 makes the estimate that the component count for the drive circuitry alone of an LSM with less than 256 words in which writing is done by the inhibit/augment method will be less than that for a CCM of the same storage capacity.

Furthermore, it is not unlikely that the form of the address and/or the required number of words in a special purpose computer or control system would be such that the decoding advantages of the CCM are as outstanding as they are when the problem requires the largest memory possible.

Step 3--Block Diagram of Memory and Memory Operation

Three highly interrelated steps lead to a detailed memory block diagram.

A. Determine the memory core layout and wiring scheme.

B. Determine the decoding scheme in terms of combinational logic and the arrangement of drivers and switches. The types of elements to be used in the drivers and switches should also be considered, and the choice made between the use of transistors, switch cores, mechanical contacts, etc.

C. Determine the mode of operation and the relative timing of events in the memory cycle. If the design is for an LSM, the method of writing should be decided upon; for cycle times on the order of five microseconds or more, writing with augmenting currents will probably prove most satisfactory. For a coincident current memory, one must decide whether or not to use such techniques as staggered read currents or post-write disturb in order to improve the signal to noise ratio.

Step 4--Signals and Signal Constraints

It is necessary to ascertain the following before working on the electronic implementation of the block diagram.

A. The input current tolerance relationships in terms of I_D/I_{sm} should be found for the memory configuration as was done in numerous examples in Chapter 5.

B. The required current pulse shapes for reading and writing and the nature of the back voltages which will occur on the drive lines as a result.

C. The nature of the memory output signals in terms of noise components and polarities.

Step 5--Driver and Switch Circuit Configurations

It is now possible to specify, or tentatively specify, circuit configurations for the drivers and switches which will produce the required currents.

Step 6--Major Circuit Elements

The three substeps here are highly interrelated with the first heavily influencing the latter two.

A. Core selection following a procedure similar to that indicated in Section 4.5.

B. Selection of transistors or other switch elements to be used in the drive circuitry. They must be capable of producing the required drive currents for the selected core.

C. Sense amplifier specification in terms of magnitudes of one and zero outputs and in the functions it is to perform.

The goal of this step is to select a core that will allow economical drive circuits and still provide a fairly uniform and easily detectable output over the extremes of operating conditions.

Step 7--Electronic Implementation of Block Diagram

The necessary circuitry to operate the memory is now

designed and/or specified.

A. The drivers and switches are designed to meet the core input current requirements and to be operable from the logical input signals.

B. Timing circuitry (which would normally be comprised of multivibrators, pulse generators, delay lines and the like) is commercially available, and the design of suitable circuitry is covered in many electronics texts.

C. The sense amplifier may be further specified in terms of the logic it is to operate and the timing circuitry which controls it. A commercial sense amplifier could be selected from this specification, or a special one could be designed.

Step 8--Breadboard and Testing

The circuitry designed is assembled, tested and evaluated.

Step 9--Finalize Design

From the results of step 8, whatever modifications are necessary are made.

9.2 Design Example

In order to illustrate the design procedure of the preceding section, an example of the design of a core memory (up to the breadboarding stage) for a special purpose digital system is now presented.

The memory to be designed is a very small and low speed one. This example was selected specifically to illustrate that a core memory is economically feasible for the specifications as well as to further illustrate the simplifications that can result for small, low-speed core memories.

It is assumed that a digital process controller is being designed, and that the design calls for a memory of specifications listed below in Step 1.

Step 1--Problem Statement

1. Purpose--The memory is to be used in a process controller.

2. Storage Capacity--Twenty words with each word containing 10 bits of information is required.

3. Temperature Environment--A commercial environment with temperature extremes of 25° to 40° C is anticipated.

4. Speed Requirements--The cycle time is to be from 8 to 15 msec, and the length of the cycle is to be controlled by the

external logic circuitry. The access time is to be 2 msec or less. Furthermore, read/write cycles occur at a rate of less than one per 50 msec.

5. Address Form--The address is to be contained in a five bit counter in which the four least significant bits is 8421 binary-coded decimal and the most significant bit has the weight of 10.

6. Logic Signals--The input levels from the counter are 0 ± 0.5 V. and -10 ± 1 V., and the control pulses have amplitude of -10 ± 1V., a minimum width of 8 μsec., and a maximum rise time of 2 μsec. The output pulses are to be positive going with a minimum amplitude of -10 V. and a minimum duration of 3 μsec.

7. Power Supplies--A -12 V. and a +6 V. are available, and both are regulated to less than 0.1% over the operating temperature range.

Step 2--Memory Form

For the small storage capacity required, an LSM is clearly indicated.

Step 3--Block Diagram of Memory and Memory Operation

A. Core Layout and Wiring--Because the operating speed is very low, the use of a single information wire per bit will present

no problems. Thus, the cores may be laid out in a 20 x 10 array with an information winding and an address winding threading each core. For the same reasons, it will not be necessary to provide impedance terminations for the drive windings. The relative orientation of the cores will be decided once the decoding scheme and mode of operation have been considered.

B. Decoding--Table 9-1 shows the twenty states of the address register. The Boolean variables V, W, X, Y, Z represent the states of the five flip flops from the most significant bit to the least significant bit respectively. There are several possible ways to perform the one out of 20 selection.

It is first noted that reed switches (which typically have a pull-in time of less than 1 msec.) fit the speed requirements. Since these devices are quite inexpensive, they are tentatively selected for use in the decoding circuitry.

The possibility of connecting the addressing lines to form a matrix for decoding purposes is now considered. The 20 address lines can be arranged to form a 4 x 5 matrix. If a scheme such as the one in Fig. 8-3 is used, then a minimum of (4 x 2) + 5 = 13 switches plus two address current drivers are required. A scheme such as the one in Fig. 8-4 would require 4 + 5 = 9 switches plus 9 address current drivers. The possibility of using extra drive wires

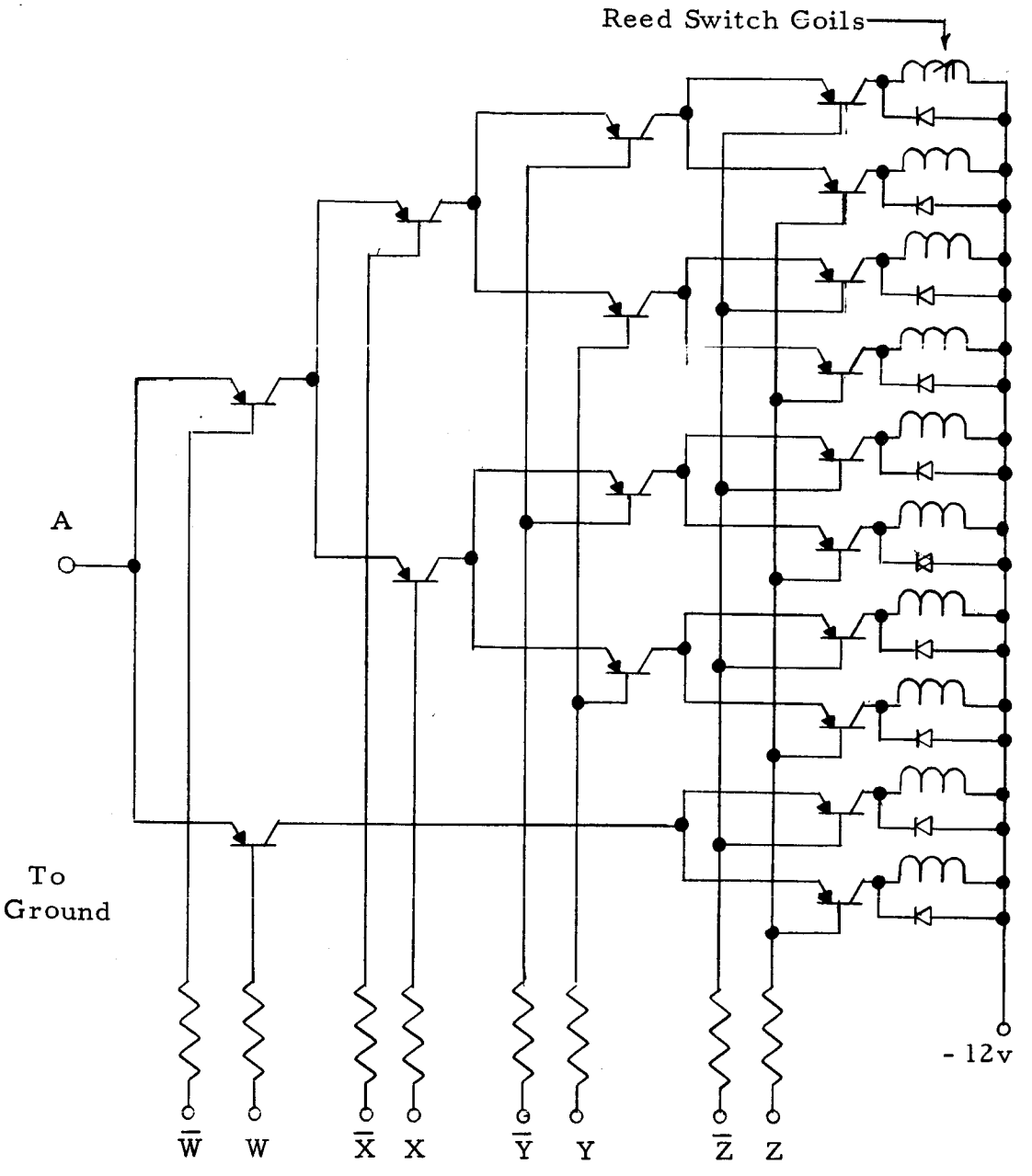
Table 9-1 States of the Address Register

Address	V	W	X	Y	Z
A_0	0	0	0	0	0
A_1	0	0	0	0	1
A_2	0	0	0	1	0
A_3	0	0	0	1	1
A_4	0	0	1	0	0
A_5	0	0	1	0	1
A_6	0	0	1	1	0
A_7	0	0	1	1	1
A_8	0	1	0	0	0
A_9	0	1	0	0	1
A_{10}	1	0	0	0	0
A_{11}	1	0	0	0	1
A_{12}	1	0	0	1	0
A_{13}	1	0	0	1	1
A_{14}	1	0	1	0	0
A_{15}	1	0	1	0	1
A_{16}	1	0	1	1	0
A_{17}	1	0	1	1	1
A_{18}	1	1	0	0	0
A_{19}	1	1	0	0	1

as in Fig. 8-5 is excluded from consideration since the use of bidirectional switch elements has been postulated and the required number of these switches is not reduced in comparison to the scheme of Fig. 8-3.

These two methods require two diodes per address or 40 diodes. If one switch per address is used as in Fig. 8-2, then no such diodes are required. Fig. 9-2 shows an 8421 BCD transistor decoding tree[2] in which the coils of the reed switches (which typically have a dc resistance of 500 ohms) are connected in series with the collectors of the 10 output transistors. With the component values shown the circuit will operate under the given signal constraints. The diodes shown protect the transistors when the current through the corresponding coil is shut off, and they would be necessary in any method employing reed switches. Point A would normally be returned to ground. Fig. 9-3 shows how two such trees may be interconnected to give the desired one-out-of-twenty selection. The "switch enable" input would normally be held at ground to prevent the switches from operating when the memory is not in use and hence to prolong their lives.

The 39 transistors required here can easily be obtained for the price of the 40 diodes required in the previous methods. The cost of the extra reed switches and their associated diodes



All inputs are negative true.
All transistors are 2N404.
All diodes are IN456.
All resistors are 608K.

Fig. 9-2 8421-BCD Decoding Tree for Selecting Reed Switches

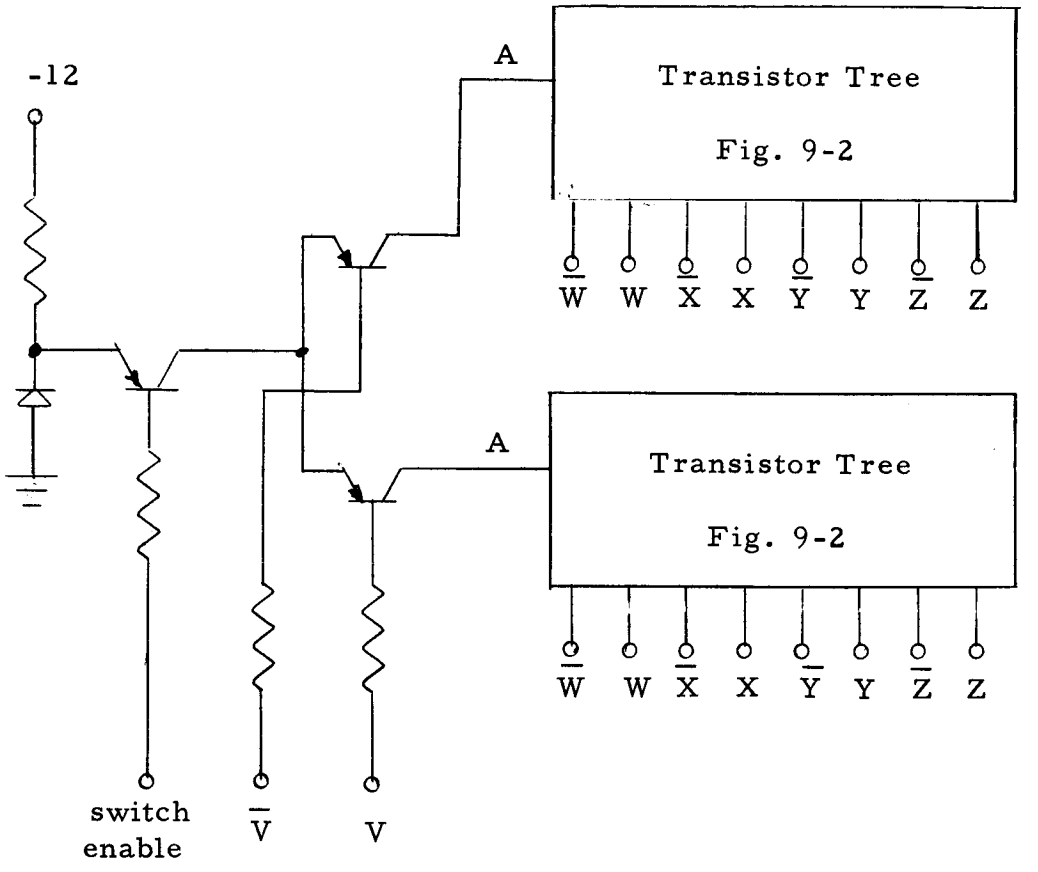


Fig. 9-3: Connection of Two 8421 BCD Trees to Perform a 1-out-of-20 Selection.

required is equivalent to or less than the cost of the logic to select the switches in the other forms.

The latter method should prove to have the longest life of the three since each switch is operated fewer times than in the other two. In order to estimate the life, note that a switch is operated once every 50 millisec in the latter method. Thus, 20 switches are operated in one second. Any given switch is then operated once a second or 3600 times an hour on the average. A conservative estimate of the minimum life of a reed switch is 36×10^6 operations. Thus, a given switch should last for 10^4 hours of operation (or for more than a year if the memory is in continual operation). Note that in the matrix methods, some switches would be operated at least four times more often to give a minimum life of 2500 hours (or on the order of three months under continual operation).

Thus, the latter method of one switch per address is chosen.

C. Mode of Operation--Writing by augmenting currents is decided upon since it gives fairly loose tolerances and should result in a fairly simple information driver design. The sequence of events in a read/write cycle is as follows:

1. The address is inserted in the address register, and

the buffer is cleared.

2. The read signal is generated and it must

(a) provide a level of -12 V. lasting for the desired length of the cycle to hold the switch enable transistor on.

(b) be delayed approximately 1.5 msec to allow the selected switch to pull in prior to causing a read current pulse to be generated.

3. After reading and the information to be written has been inserted into the buffer, the write signal is generated which causes the information to be written.

It is now tentatively decided that the read current source and the information current drivers will derive their current from the -12 volt supply, and that the addressing current for writing will derive its current from the +6 volt supply.

The above decisions are summarized in the block diagram of Fig. 9-4, which shows the cores in their proper orientations for the current directions decided upon.

Step 4--Signals and Constraints

A. The input current tolerance relationships for this memory are given in Section 5.3.3 by equations (5.3.4), and (5.3.6) through (5.3.11). Also the curves in Figs. 5-7 and 5-12

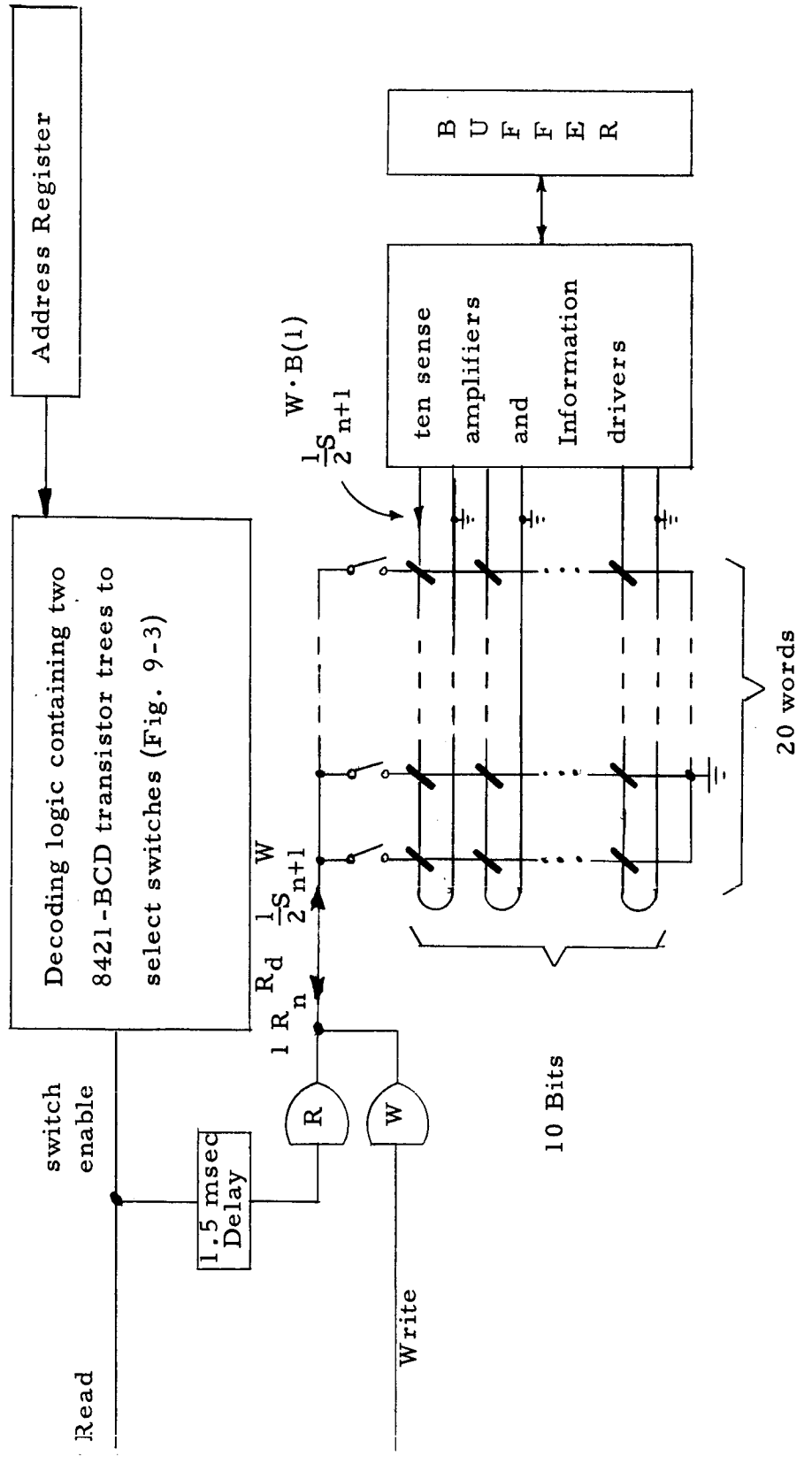


Fig. 9-4: Initial Block Diagram of Memory Being Designed

may be employed. It is assumed that desirable tolerances for the information currents and write addressing current are ten and five percent, respectively.

B. The current pulse shapes for writing are not at all critical because of the low speed. The read current should have a rise time that conforms to the core manufacturer specification. During the read operation, the back voltage on the drive line should be less than two volts if the cores have a UV_1 of less than 200 mv each.

C. From the block diagram it is clear that the outputs from the core array will be positive with respect to ground during read. Because the read current may be made very large, it is expected that a DV_Z output will be several times smaller than a UV_1 output. Also the only major source of noise will be due to reading a zero since the drive lines are well isolated from one another by means of the reed switches.

Step 5--Driver and Switch Circuit Configurations

The reed switch drive circuitry was decided upon in Step 3A as a justification for the method of decoding. There have been no further decisions made that necessitate a change in that circuitry.

The information current driver configuration in Fig. 6-6 appears to be suitable for the information drivers required here,

and the current driver configuration of Fig. 6-14 is suitable for the read current driver.

For the write addressing current driver, a simple transistor switch may be used since the waveshape is not important. The configuration of Fig. 9-5 is proposed, which requires a negative-going input transition to activate it.

Step 6--Major Circuit Elements

Most any commercially available core would be workable in this memory. However, the core finally selected should allow economy in the drive circuitry, and it would be desirable that the UV_1 output be as large as possible so that the gain requirements of the sense amplifier would be minimized, which implies that the thermal stability of the amplifier would be enhanced by allowing more negative feedback.

In order to keep the cost of the drive circuitry low, the use of low cost silicon transistors wherever possible is proposed. This implies that full select currents may be on the order of 400 to 600 ma.

The above considerations pretty well limit the search for a core to those of the 50 and 80 mill sizes. With drive currents in the range indicated, it is found that cores of the 80 mill size with switching times on the order of one micro-second produce the

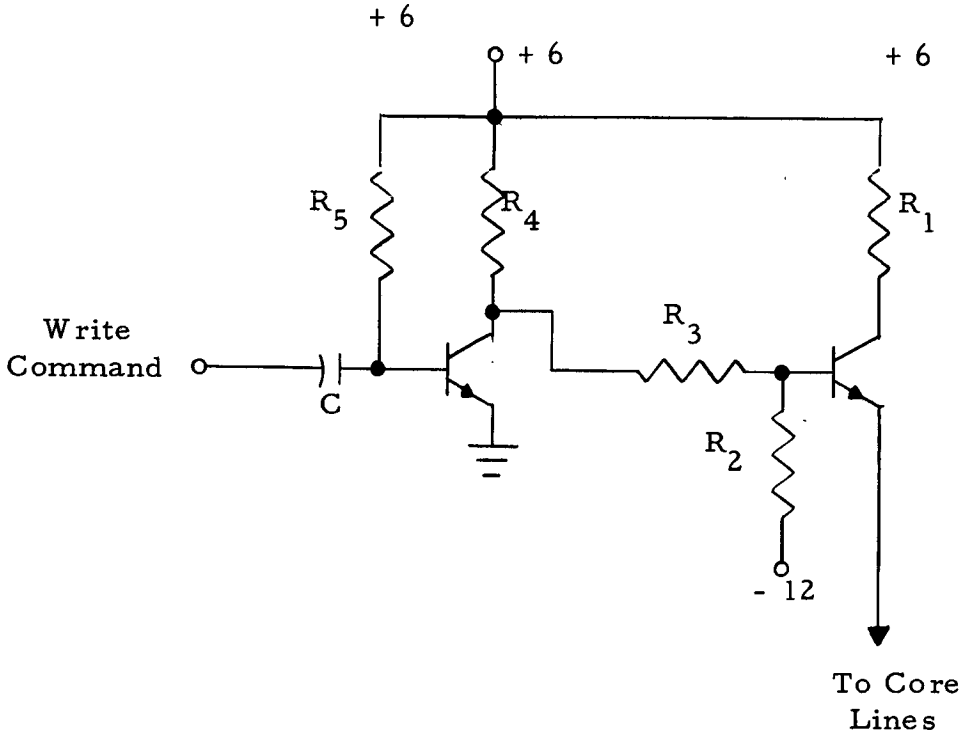


Fig. 9-5 Proposed Write Addressing
Current Driver

largest outputs, and the choice among these cores is small. Two examples--both manufactured by Indiana General Corporation--are the MC 113, which produces a UV_1 of 100 mv at a current of 740 ma, and the MC 169, which produces 120 mv at 560 ma. Of these two the latter appears to be best suited since it gives a larger output at a smaller current than does the former. The performance of the MC 169 is now investigated over the operating temperature range of 25° to 40° C in a manner similar to that of Section 4.5.

Recall from Chapter 5 that the information current with tolerance is expressed as $I_I\ (1 \pm \Delta_I)$, and that write addressing current with tolerance is $I_W\ (1 \pm \Delta_W)$.

For $\Delta_I = 0.10$ and $\Delta_W = 0.05$, the necessary I_D/I_{sm} is 0.58. Recall that this determines I_{sm} at the highest operating temperature. From the specification sheet for the core, it is estimated that at 40° C, I_D/I_{sm} is greater than 0.58 at a current of 567 ma, and at this current the core still switches satisfactorily at the low temperature of 25°C. Thus, this value of I_{sm} is usable over the temperature range. I_D is then found as

$$I_D = (I_D/I_{sm})\ (I_{sm}) = 0.58 \times 567 = 330 \text{ ma.}$$

Using the equalities in relations (5.3.7) and (5.3.8), the nominal values of I_W and I_I are found

$$I_W = \frac{I_D}{1 + \Delta_W} = \frac{330}{1.05} = 315 \text{ ma}$$

$$I_I = \frac{I_D}{1 + \Delta_I} = \frac{330}{1.10} = 300 \text{ ma}$$

The switching speed of the core at a current of I_{sm} = 567 ma is 1.1 μsec at 25° C with a current rise time of 0.2 μsec. With this rise time, this will be the longest switching speed encountered. Since the write current drivers will have longer rise times, the write current pulse widths are specified to be greater than 5 μsec.

The specification also shows that UV_1 is greater than 150 mv and the switching time less than 1.1 μsec for a full read current greater than 600 ma. The rise time of the read current should be in the neighborhood of 0.2 μsec which gives a DV_Z response of less than 35 mv. Since good discrimination in the output is achieved at this read current, the output of the read driver is specified to be a pulse with an amplitude greater than 600 ma, a rise time of 0.2 μsec, and a width greater than 2 μsec; and the sense amplifier must accept positive pulses of amplitude greater than 150 mv, and reject pulses of amplitude less than 35 mv. (The input signal to the read driver and the output signal of the sense amplifier have been specified in the problem statement).

Thus, the required drive currents allow the use of

economical transistors, and the output voltage will allow the use of a simple and inexpensive amplifier such as the one in Fig. 7-2.

It is, therefore, concluded that this core is very well suited to the application, and this core is selected for use.

The transistors for the core drivers are now chosen. For the NPN transistors in the read current source and for the output transistor of the write address current driver the 2N3704 is selected. For the output transistors of the information drivers, the PNP 2N3638 is selected. Both silicon transistors are suitable for use as high current switches. The ac coupled input stages of the write current drivers require transistors with fairly high gains and high base-emitter breakdown voltages. Thus, the germanium 2N1308 NPN transistor is selected for use in the write address current driver, and the germanium 2N1309 PNP transistor is selected for the information drivers.

Step 7--Electronic Implementation

A. Drivers--The write address current driver is considered first, and it is found that it is impossible to produce the desired I_W. To show why note that the collector emitter saturation voltage for the silicon transistor could vary from 0.2 to 1.0 volts at the collector current in question. (The power supply voltage varies less than 0.06 volts, and this variation is negligible for now).

Neglecting the base current for the moment, the output current is

$$I_W = \frac{6 - V_{CE}(sat)}{R_1}$$

The limits on R_1 are now found

$$I_{W_{max}} = 315\,(1 + 0.05) = \frac{5.8}{R_{1_{min}}}$$

$$\text{or } R_{1_{min}} = 17.5 \text{ ohms}$$

Similarly

$$I_{W_{min}} = 315\,(1 - 0.05) = \frac{5.0}{R_{1_{max}}}$$

or

$$R_{1_{max}} = 16.7 \text{ ohms}$$

Because $R_{1_{max}}$ must be less than $R_{1_{min}}$, there is no value of R_1 that can be used.

Because of the relatively large range of values that $V_{CE}(sat)$ can take on in comparison to the power supply voltage, it is necessary that a larger tolerance in I_I be allowed. This may necessitate that Δ_I be made smaller for the core to still operate

reliably. Thus, the core must be re-evaluated in Step 6. One of the following three possible conclusions must be reached

1. The core may still be operated with Δ_I remaining as 0.10, but with a new Δ_W that allows realizable current driver conditions.

2. The core may still be operated, but with Δ_I decreased slightly to give the proper Δ_W.

3. The core may be operated only if Δ_I is reduced to an objectionally low value for economy (say less than 0.07).

Clearly, the first of the three would be the most desirable solution. Thus, the core is evaluated keeping $\Delta_I = 0.10$ for different values of $\Delta_W > 0.05$. Following each try at a new Δ_W, the results for I_W are to be analyzed as to their realizability.

It is found that if $\Delta_I = \Delta_W = 0.10$, then the necessary I_D/I_{sm} is 0.61. The specification sheet gives $I_{sm} \approx 540$ ma at 40°C as a conservative figure. Then I_D is close to 330 ma (this is the same I_D as before which implies that the core is still operating on the major loop at 40°C), and as a result $I_I = I_W = 300$ ma. At 25°C the core still switches satisfactorily at 540 ma so that these currents are still usable as far as the core operation is concerned.

With $I_W = 300$ ma and $\Delta_W = 0.10$, it is found that the limits on R_1 are (again neglecting the base current) $17.5 < R_1 < 18.5$

ohms, which (if precision resistors are used) should give a realizable driver. Note that this has not effected the conditions for the read driver and sense amplifier.

Further attempts at increasing Δ_W (keeping Δ_I fixed) would further reduce I_{sm} and the low temperature switching at I_{sm} would begin to become marginal. Thus, this operating point for writing just found will be tried in an attempt to design the write address current driver. The switching time has not changed appreciably from the original operating point, so the minimum pulse width specification has not been changed from 5 μsec.

Unfortunately, it is found that because the base current is part of the output current and is effected by the three resistors R_2, R_3, and R_4 as well as large possible variations in the base-emitter saturation voltage, the output requirements cannot be achieved. It is recalled, however, that in the configuration of Fig. 6-6 there is only one resistor effecting the base current. Therefore, this configuration is tried (with NPN transistors and a positive supply voltage) and found to produce the desired output.

The design follows the outline given in Section 6.3.2. A problem arises in the timing circuit since if the initial base voltage of the input transistor is +1 volt, and if the negative going input transition is 10 volts in magnitude, the transistor will not be cut off.

To solve the problem a -3.2 ± 5% volt reference is established for the emitter using a 3.2 V Zenner diode to ground and a resistor to the -12 V supply. The resultant circuit is shown in Fig. 9-6. The one percent resistors are metal film ones, and the capacitor was selected to give a pulse width greater than 5 μsec.

The information drivers are to use the configuration of Fig. 6-6. Following the method of Section 6.3.2 the components listed in Table 9-2 are arrived at to give the desired output current of 300 ± 10% ma and a pulse width greater than 5 μsec.

Table 9-2 Components for the Circuit of Fig. 6-6 to be used in the design example

Component	Value
R_1	43Ω, 5%, 1W
R_2	330Ω, 5%, 1/2 W
R_3	100Ω, 10%, 1/2 W
R_4	15K, 10%, 1/2 W
C	0.0015 μf
Q_1	2N3638
Q_2	2N1309

For the read driver, the circuit of Fig. 6-14 with component values as listed in Table 6-2 should work directly with no

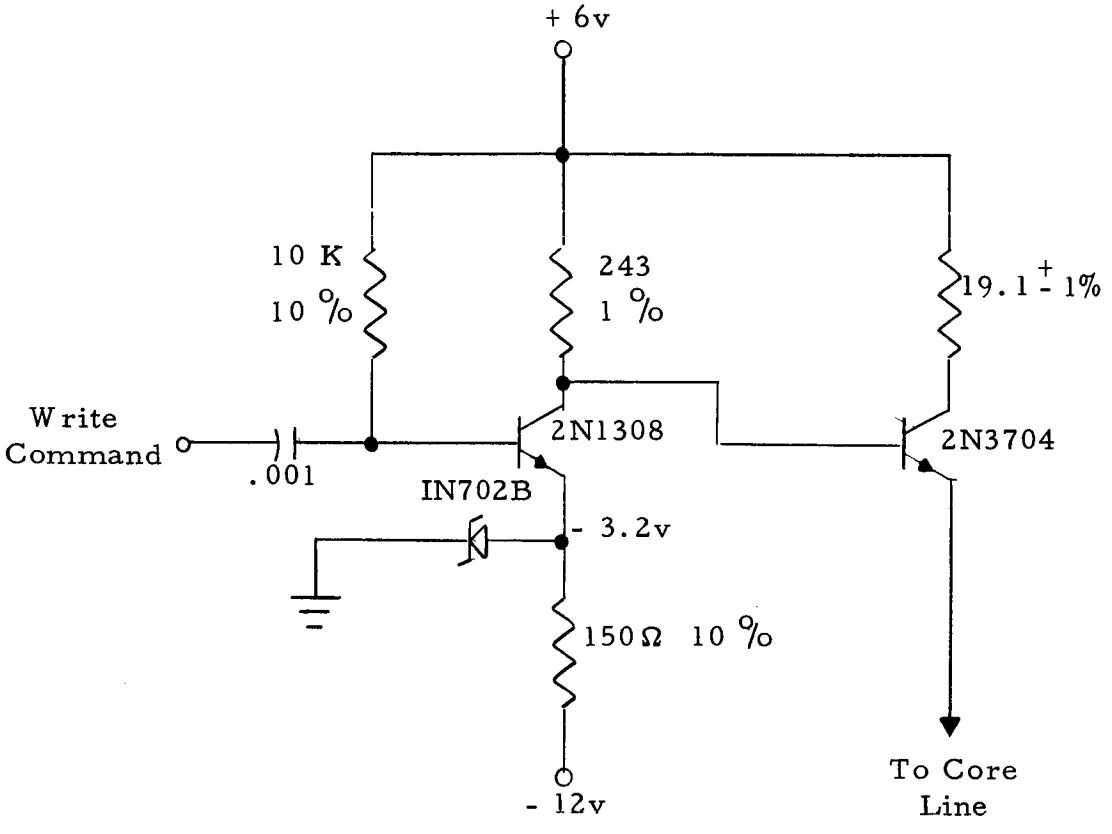


Fig. 9-6 Final Design of the Write Addressing Current Driver

problems since these values meet the design conditions of a current amplitude greater than 600 ma. However, during the bread board and testing phase of the design, it may be necessary to adjust the values of the capacitors; and the possibility of using the -3.2 volt reference established in Fig. 9-6 for $-E_3$ should be considered.

The sense amplifier of Fig. 7-2 and described in Section 7.3.1 exactly meets the specifications made in the previous step. However, it has no facility for rejecting noise during the write portion of the memory cycle. Its output will therefore have to be passed through an AND gate that is enabled only during read time.

The final step to be considered is that os specifying the timing circuitry. The logic system must generate a negative going pulse as the read signal which will last the length of the memory cycle. Since this will most likely be generated by a multivibrator, the corresponding positive-going pulse may be used to trigger a 1.5 msec delay monostable multivibrator whose delayed, negative-going output transition will activate the read current driver.

The required enable signal for the AND gates at the output of the sense amplifiers will depend upon the form of these AND gates. In particular if they are a-c coupled steering gates, it

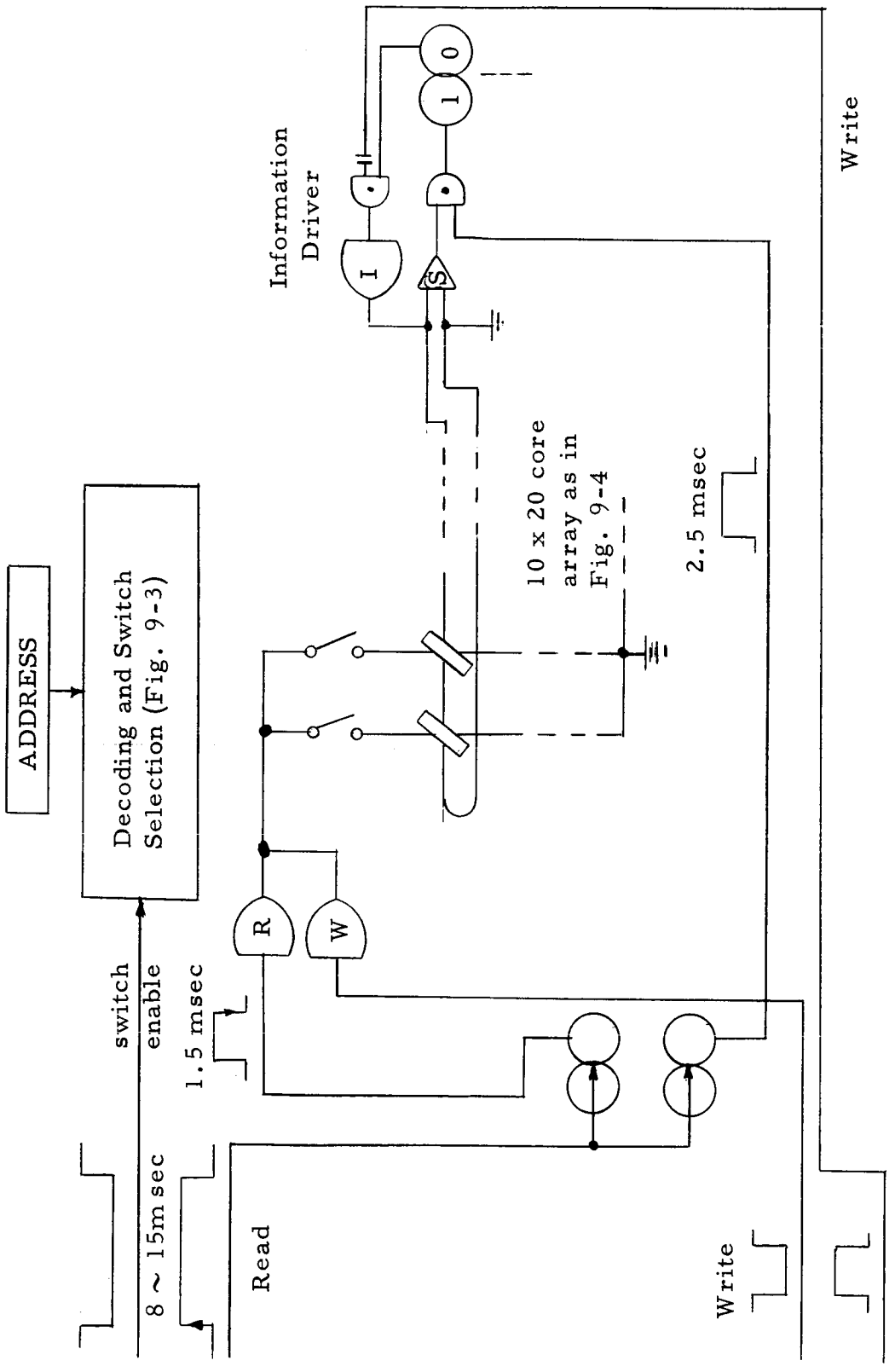


Fig. 9-7: Final Memory Design

will be necessary to provide the enable signal prior to the memory output to allow for their recovery time. Thus, a second monostable multivibrator is triggered from the positive-going read signal, and its output is used to enable the AND gates. The duration of this enable pulse is selected as 2.5 msec. to allow for variations in time delay in the first monostable multivibrator.

For writing, a negative going transition is required by the address current driver and a positive going signal is required by the information drivers. It is again assumed that the logic system generates both required signals simultaneously.

The final memory configuration is indicated in Fig. 9-7.

9.3 References for Chapter 9

1. Meyerhoff, A.J , et al., Digital Applications of Magnetic Devices, New York: John Wiley and Sons, Inc., 1960, pp. 369-370.

2. Littauer, R., Pulse Electronics, New York: McGraw-Hill Book Company, 1965, pp. 512-515.

APPENDIX

Derivation of the Number of Partially Selected Cores in a CCM Bit Plane Whose Noise Voltages are not Cancelled

In an ℓ x m CCM bit plane there are $(\ell-1) + (m-1)$ partially selected cores in a read operation. If a cancelling sense winding is used, then the noise voltages produced by these cores will tend to cancel; but there will usually be one or more cores whose noise is not cancelled by any other core. To determine the number of these cores and the polarity of their noise signals, ℓ and m are examined in terms of whether they are odd or even numbers. There are three cases to consider:

1) both dimensions are even
2) both dimensions are odd
3) one dimension is even and the other is odd

Case 1: If ℓ and m are both even, then $(\ell-1)$ and $(m-1)$ are both odd numbers; and the sum $(\ell-1) + (m-1)$ is even. Now of all the cores in the selected row there are $\ell/2$ cores which produce positive voltages and $\ell/2$ which produce negative voltages. In the selected column there are $m/2$ cores which produce voltages of the same polarity.

The selected core at the intersection of the row and column produces a voltage of only one polarity which is arbitrarily taken as positive. When the contents of this core is read, there will therefore be $(\ell/2 - 1) + (m/2 - 1)$ cores producing noise of positive polarity; and there will be $(\ell/2) + (m/2)$ cores producing noise of negative polarity. The number of cores producing negative noise exceeds the number producing positive noise by two. It is therefore concluded that there are two cores whose noise is in no way cancelled and that the polarity of this uncancelled noise voltage is negative with respect to the signal from the selected core.

Case 2: If ℓ and m are both odd, then $(\ell-1)$ and $(m-1)$ are both even numbers, and the sum $(\ell-1) + (m-1)$ is even. In the selected row there are $(\ell-1)/2$ cores producing voltages of one polarity, and $(\ell+1)/2$ cores producing voltages of the opposite polarity. In the selected column, $(m-1)/2$ cores produce voltages of like polarity.

Assuming that the signal voltage from the selected core is positive, then in the selected row either (but not both) of the following two situations may occur:

1) $\frac{\ell-1}{2}$ - 1 cores produce positive noise,

and $\frac{\ell+1}{2}$ cores produce negative noise.

2) $\frac{\ell+1}{2}$ - 1 cores produce positive noise,

and $\frac{\ell-1}{2}$ cores produce negative noise.

Also in the selected column either (but not both) of the following occur:

3) $\frac{m-1}{2}$ - 1 cores produce positive noise,

and $\frac{m-1}{2}$ cores produce negative noise.

4) $\frac{m+1}{2}$ - 1 cores produce positive noise,

and $\frac{m-1}{2}$ cores produce negative noise.

In situation 1 (or 3) there are two negative noise signals produced in the row (or column) that are not cancelled by positive

noise signals in that row (or column). In situation 2 (or 4) every noise voltage in the row (or column) is cancelled by an opposite voltage in that row (or column). Therefore, there are three possible results.

A. When situation 1 occurs with situation 3, there are four cores whose noise is in no way cancelled; and polarity of the uncancelled noise is negative.

B. When situation 1 occurs with situation 4 or when situation 2 occurs with situation 3, there are two cores whose noise is not cancelled; and the polarity of the uncancelled noise is negative.

C. When situation 2 occurs with situation 4, every noise voltage is cancelled by another noise voltage.

Case 3: If one dimension is even and the other is odd and if the polarity of the signal of the selected core is assumed positive, then from the results of the two preceding cases it is clear that the following occurs:

1) In the dimension with an even number of cores, there is alwasy one core that produces a negative noise voltage that is not cancelled by the noise of another core in that dimension.

2) In the dimension with an odd number of cores either there are two cores producing negative noise voltages that are not cancelled by the noise of other cores in that dimension or every noise voltage in that dimension is cancelled by another noise voltage in that dimension.

Therefore there is always a net negative noise voltage produced by either one or three partially selected cores whose noise is not cancelled. These results have been summarized in Table 5-1.